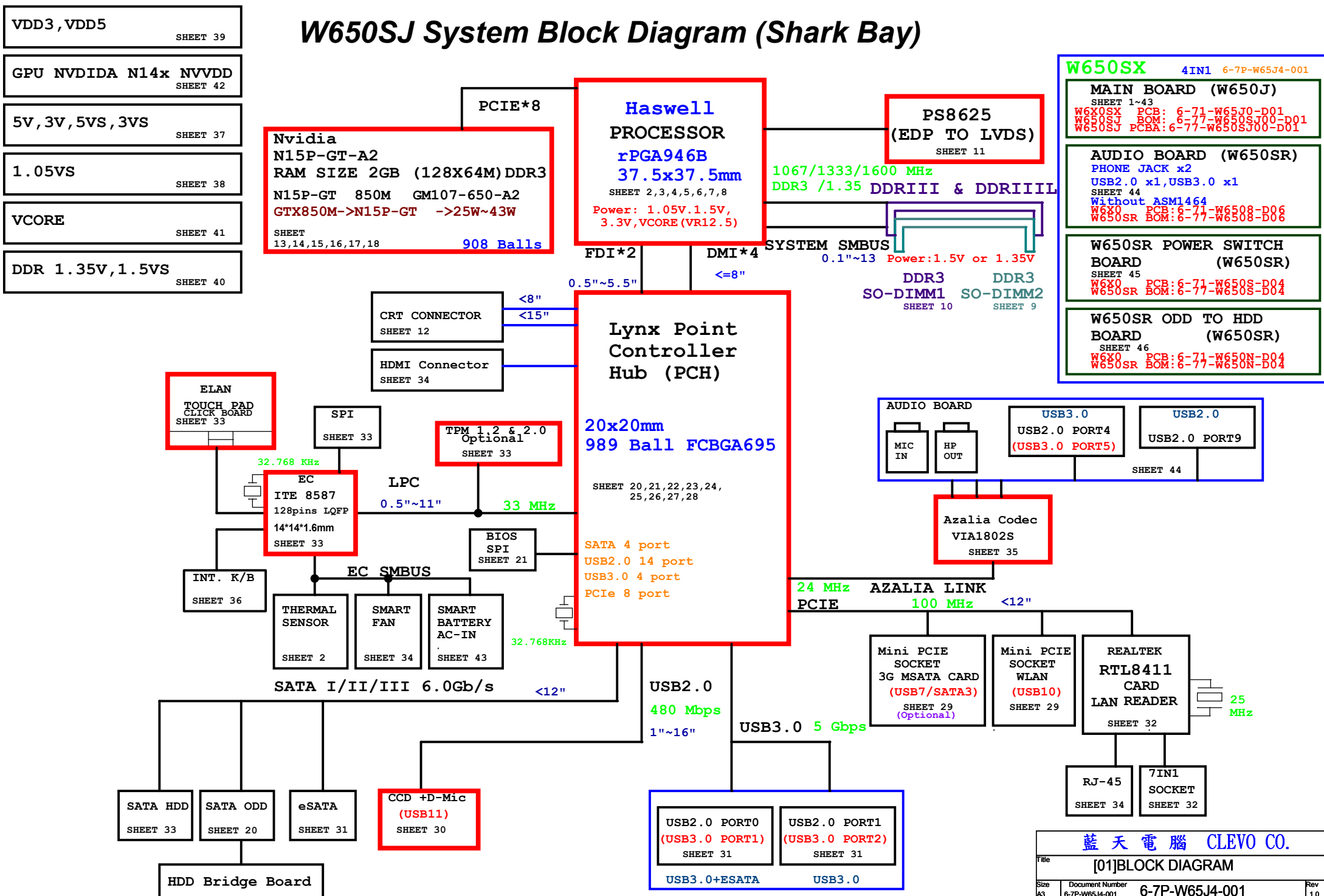
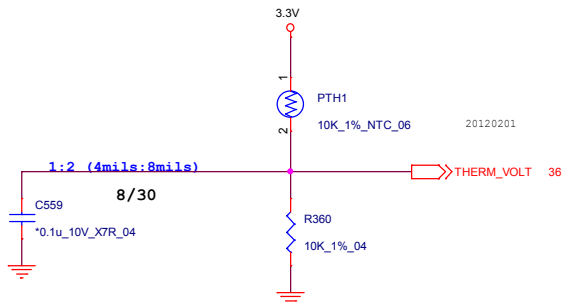
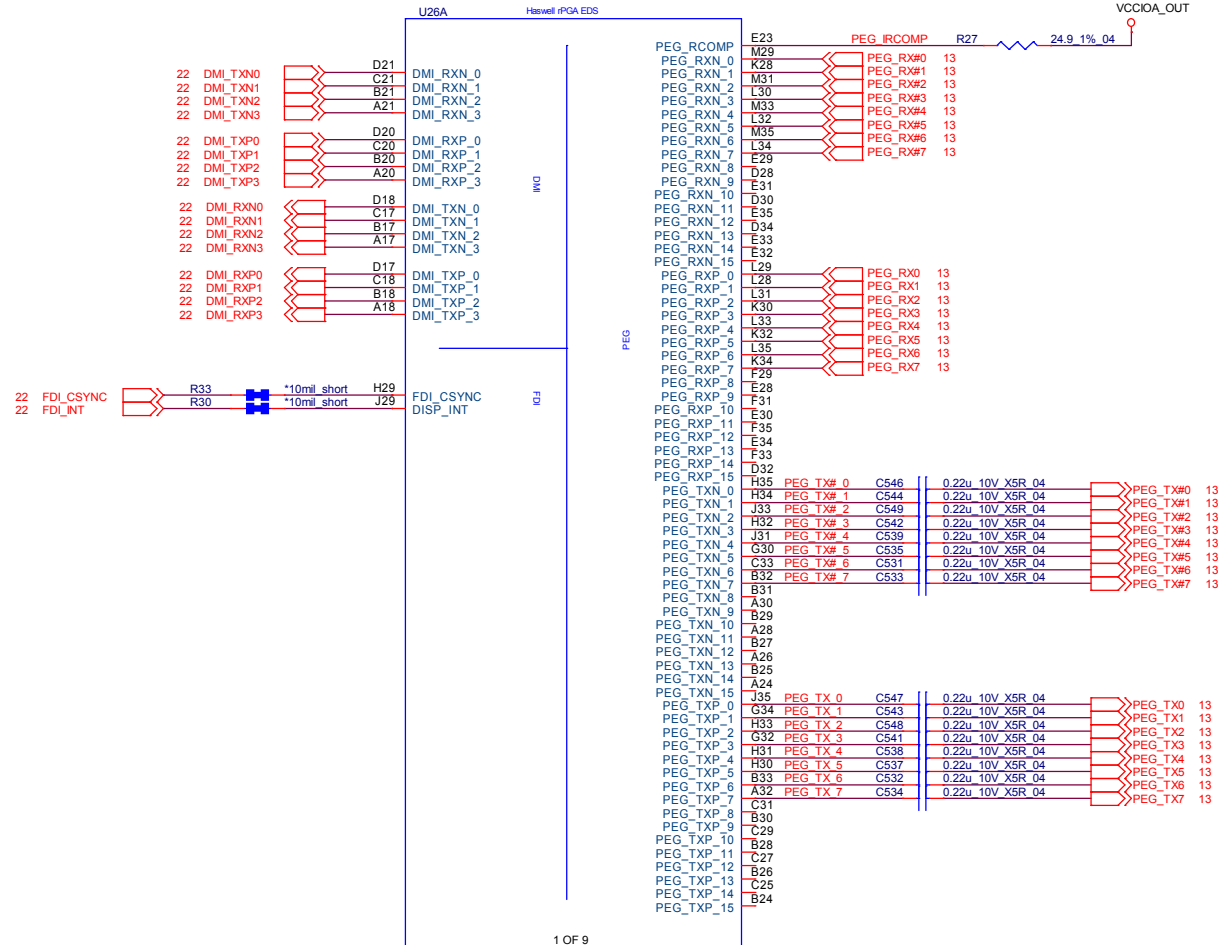
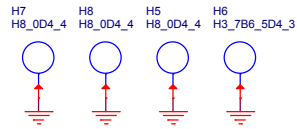


# W650SJ System Block Diagram (Shark Bay)



# Haswell rPGA Processor 1/7 ( DMI,PEG,FDI )

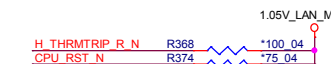
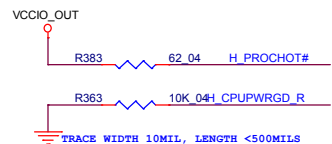
## CPU HOLD



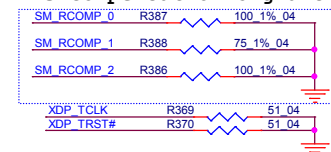
藍天電腦 CLEVO CO.

Title				
[02] Haswell 1/7-DMI/PEG/FDI				
Size	Document Number			Rev
A3	6-7P-W65J4-001			1.0
6-71-W65J0-D01				
Date:	Wednesday, October 09, 2013		Sheet	2 of 46

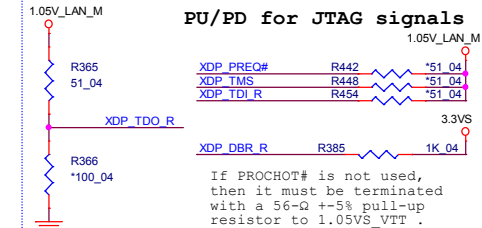
## Haswell Processor 2/7 ( CLK,MISC,JTAG )



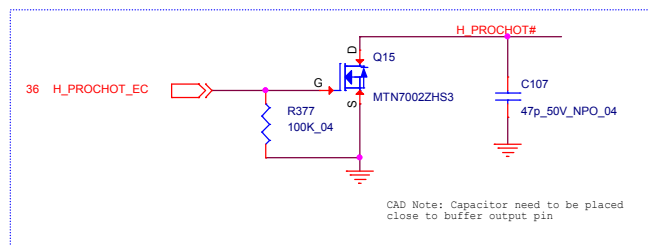
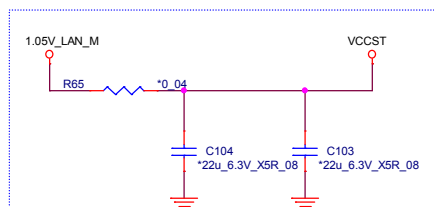
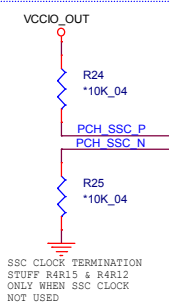
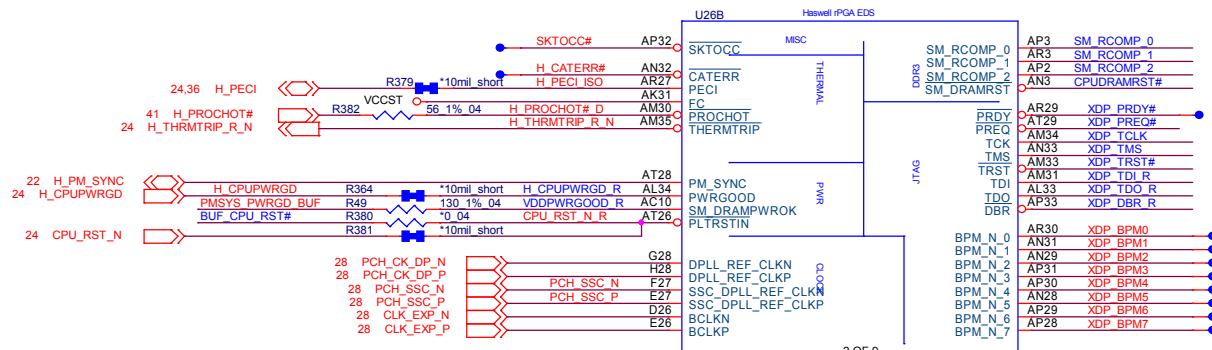
## DDR3 Compensation Signals



PU/PD for JTAG signals

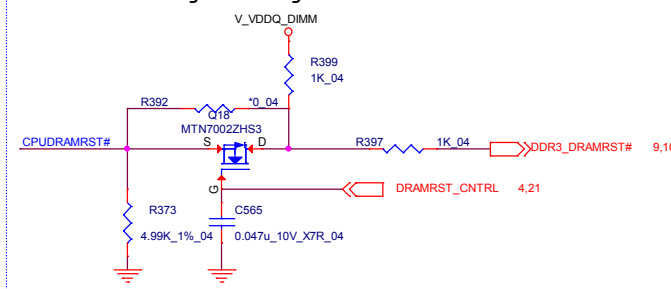


If PROCHOT# is not used, then it must be terminated with a 56- $\Omega$   $\pm$ 5% pull-up resistor to 1.05V<sub>S</sub> VTT.

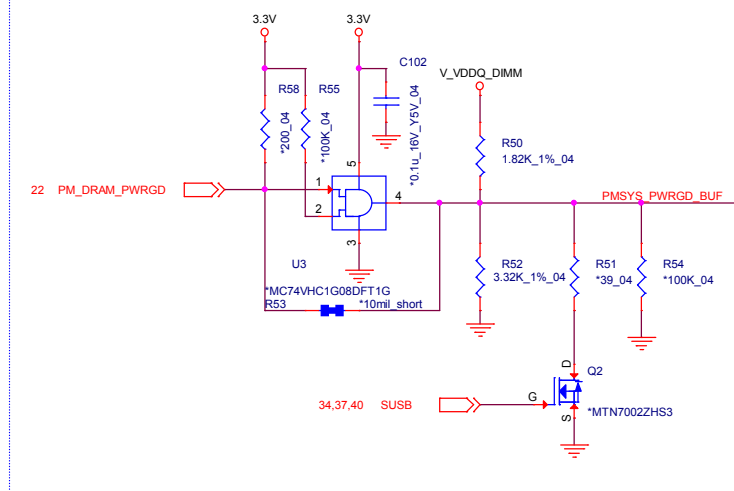


CAD Note: Capacitor need to be placed close to buffer output pin

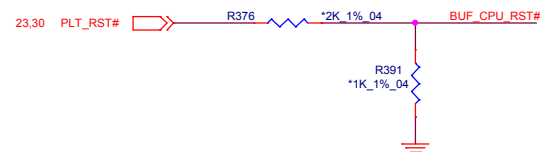
S3 circuit:- DRAM\_RST# to memory should be high during S3



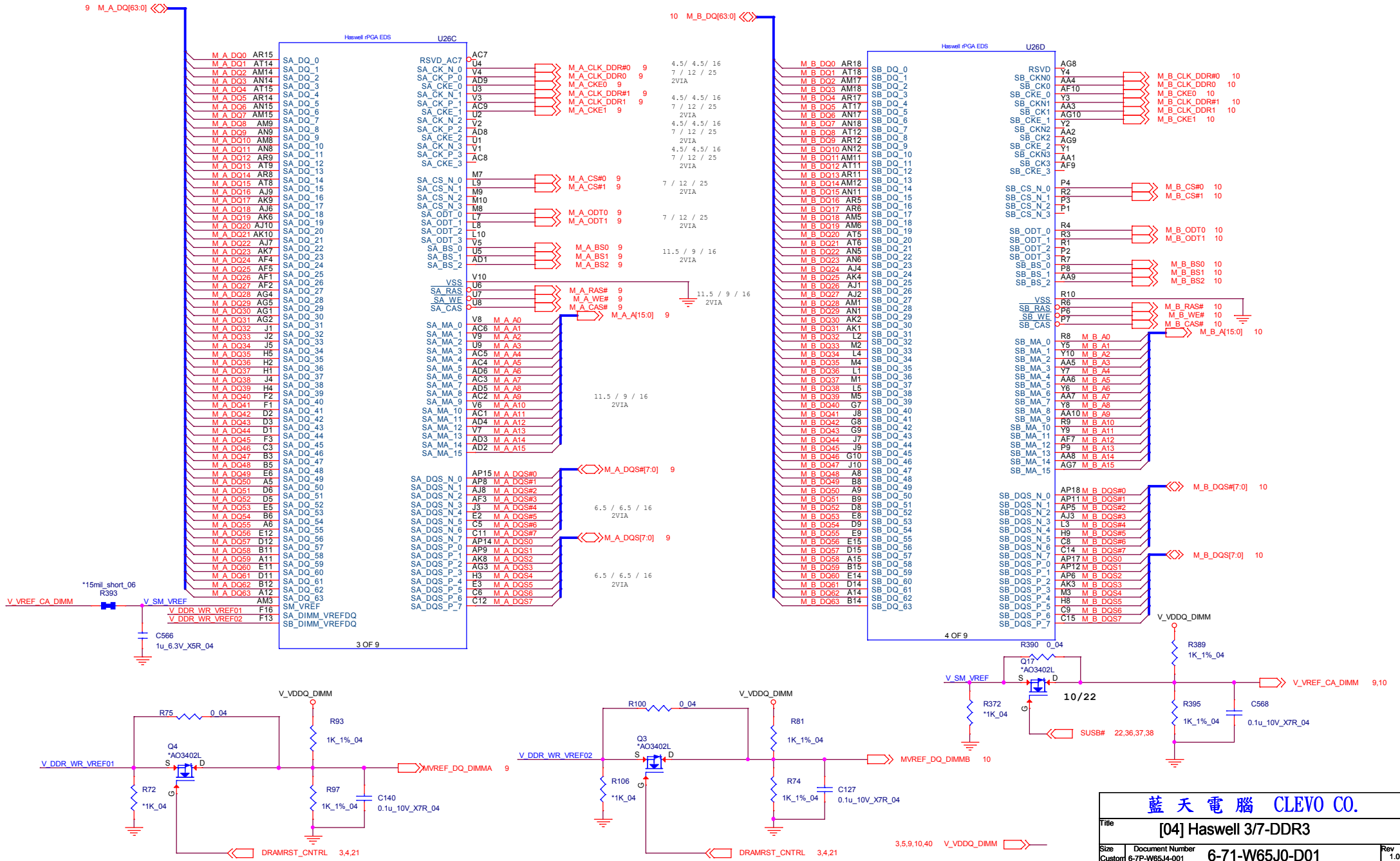
S3 circuit:- DRAM PWR GOOD 1CIRCUIT



## Buffered reset to CPU



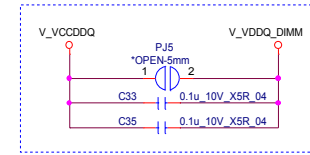
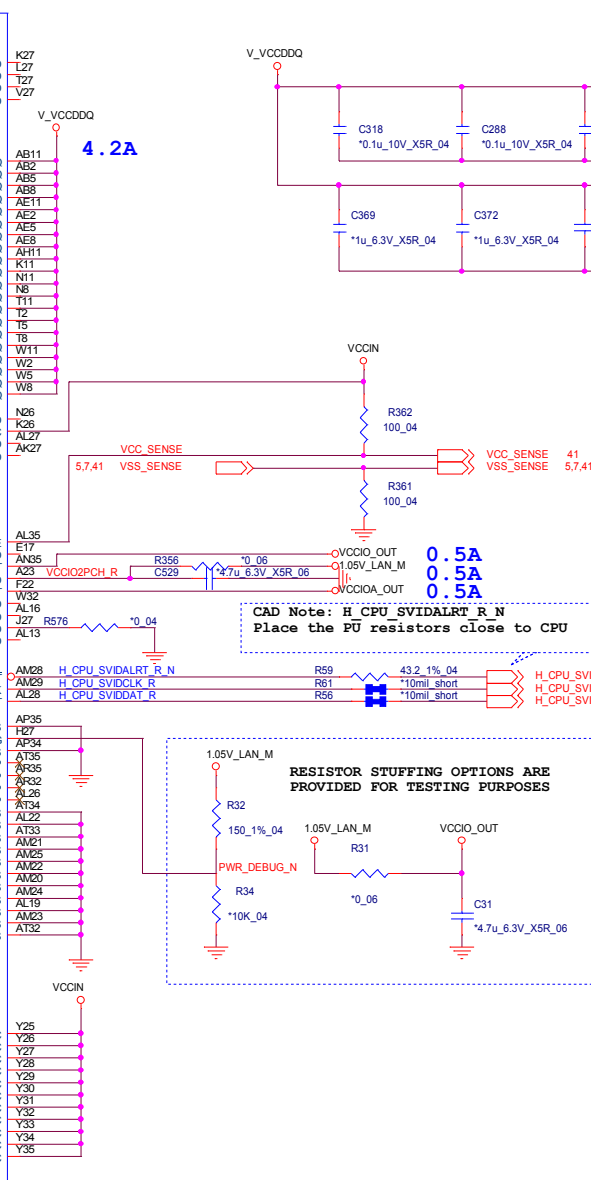
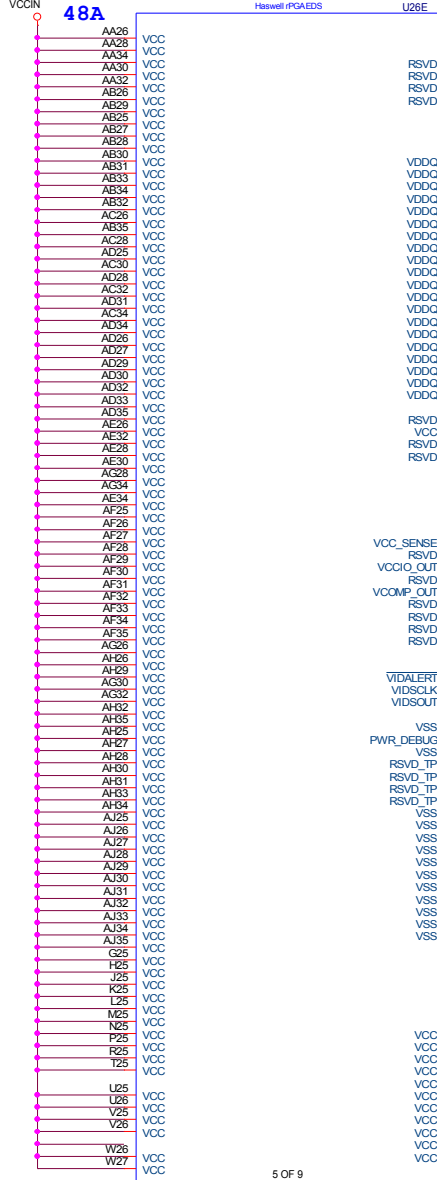
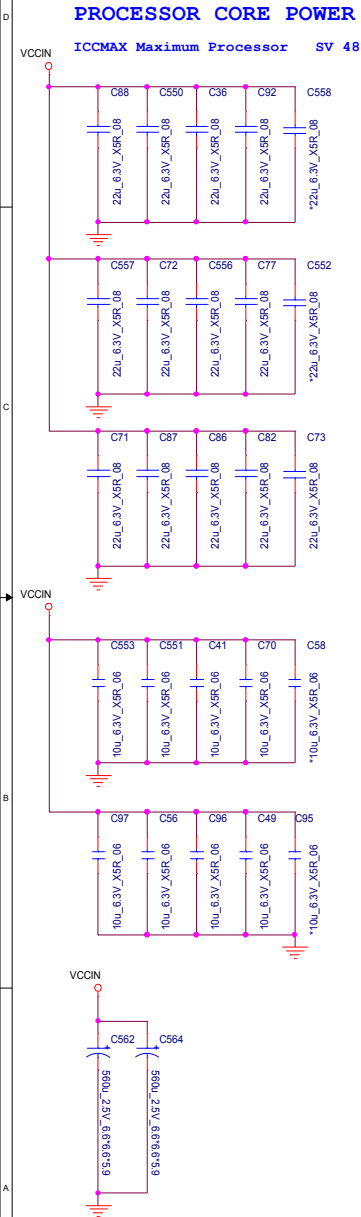
Haswell Processor 3/7 ( DDR3 )



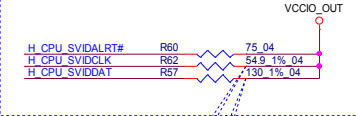
# Haswell Processor 4/7 ( POWER )

## PROCESSOR CORE POWER

ICCMAX Maximum Processor SV 48



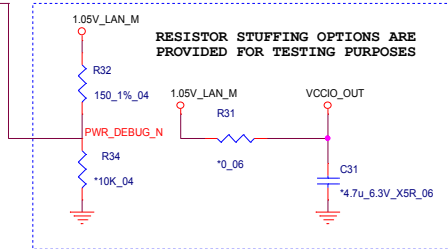
## SVID Signals



CAD Note: H\_CPU\_SVIDCLK  
PLACE THE PU RESISTORS  
CLOSE TO VR

CAD Note: H\_CPU\_SVIDCLK\_R  
Place the PU  
resistors close to VR

## RESISTOR STUFFING OPTIONS ARE PROVIDED FOR TESTING PURPOSES



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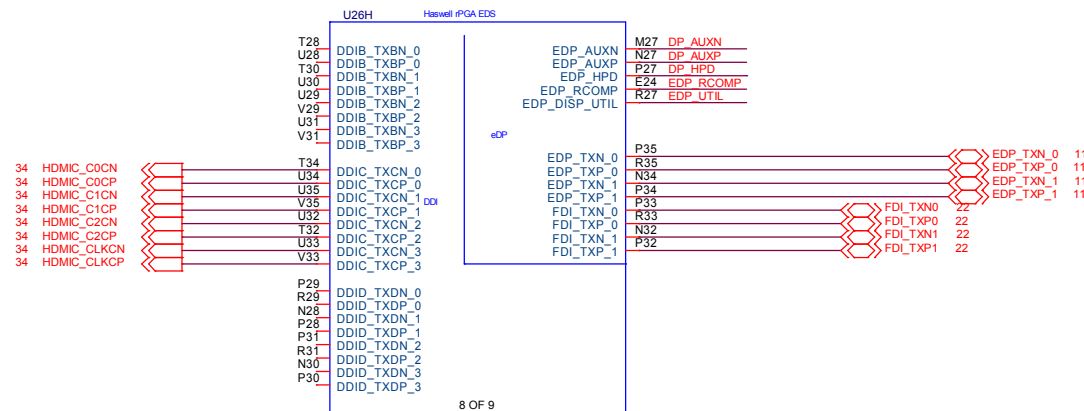
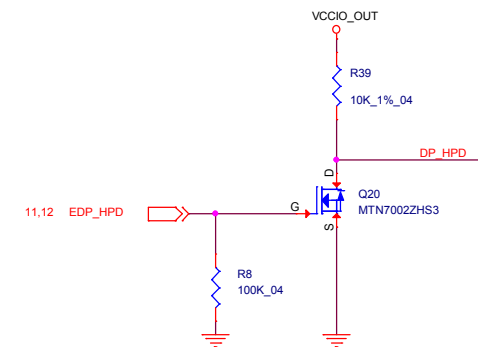
[05] Haswell 4/7-POWER

Size	Document Number	Rev
Custom	6-7P-W65J4-001	1.0
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3.6 VCCIO\_OUT  
2.8 VCCIOA\_OUT  
3.4,9,10,40 V\_VDDQ\_DIMM  
3.26,27,38,41,42 1.05V\_LAN\_M  
8.41 VCCIN

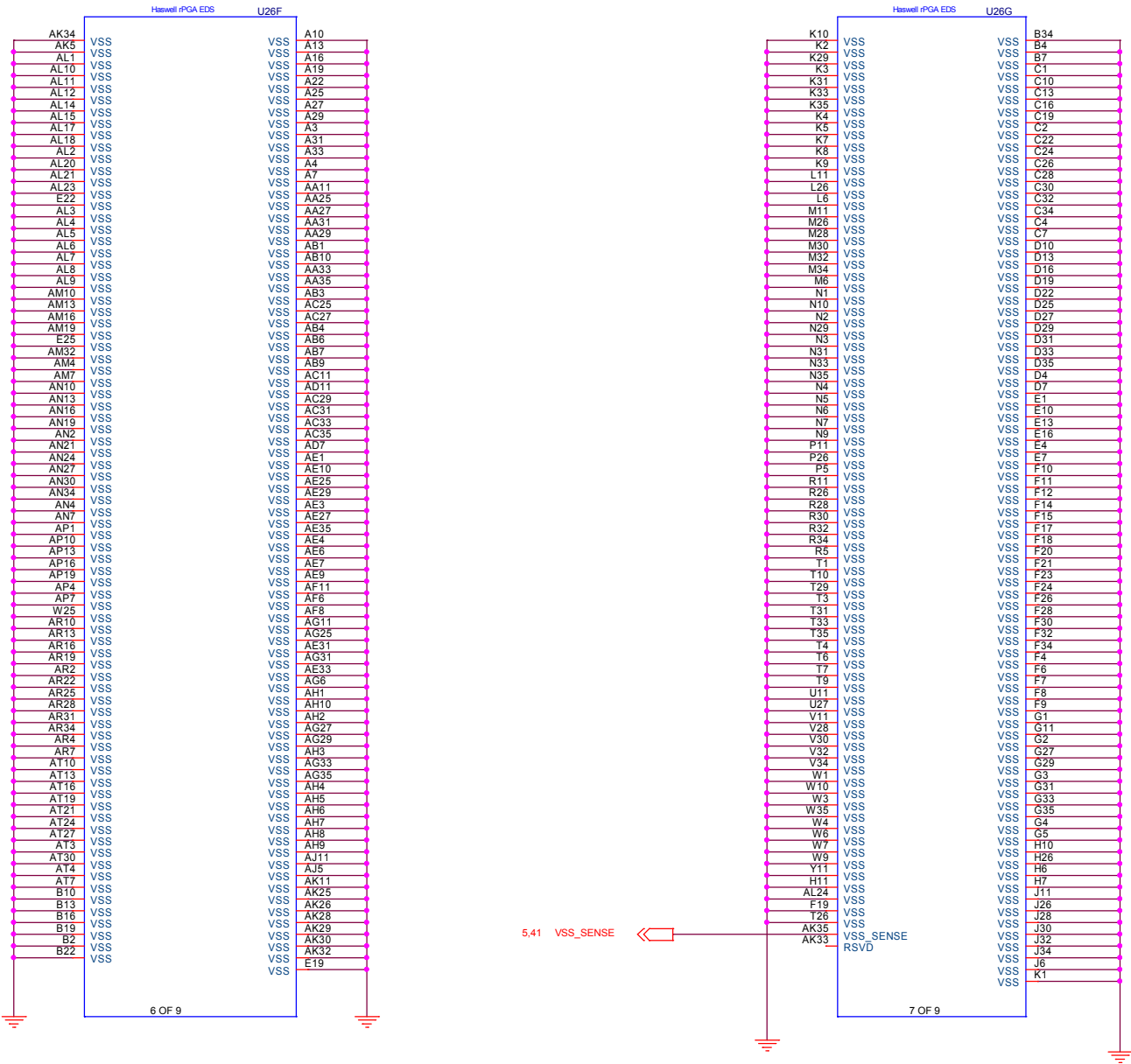
## 藍天電腦 CLEVO CO.

Size	Document Number
A3	6-7P-W65J4-001 6-71-W65J0-D01



3,5 VCCIO\_OUT  
2,5 VCCIOA\_OUT  
3,9,10,11,12,19,20,21,22,23,24,26,27,28,29,30,31,32,33,34,35,36,37,41 3.3VS

Haswell Processor 6/7 ( GND )



# Haswell Processor 7/7 ( RESERVED )

## CFG Straps for Processor

PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS

CFG2 1: (DEFAULT) NORMAL OPERATION; (Default)  
LANE# DEFINITION MATCHES  
0: LANE REVERSAL

CFG2 R66 \*1K\_04

## DISPLAY PORT PRESENCE STRAP

CFG4 1: DISABLED;  
NO PHYSICAL DISPLAY PORT ATTACHED  
TO EMBEDDED DISPLAY PORT  
0: ENABLED; AN EXTERNAL DISPLAY PORT DEVICE  
AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED  
TO THE EMBEDDED DISPLAY PORT (Default)

CFG4 R68 \*1K\_04

## PCIe Port Bifurcation Straps

CFG[6:5] 11: DEVICE1 FUNTION 1, DEVICE 1 FUNCTION2 DISABLED  
10: DEVICE1 FUNCTION1 ENABLED DEVICE1 FUNCTION 2 DISABLED  
01: DEVICE 1 FUNCTION 1 DISABLED, DEVICE 1 FUNCTION 2 ENABLED  
00: DEVICE 1 FUNCTION 1 ENABLED, DEVICE 1 FUNCTION 2 ENABLED

CFG5 R64 \*1K\_04

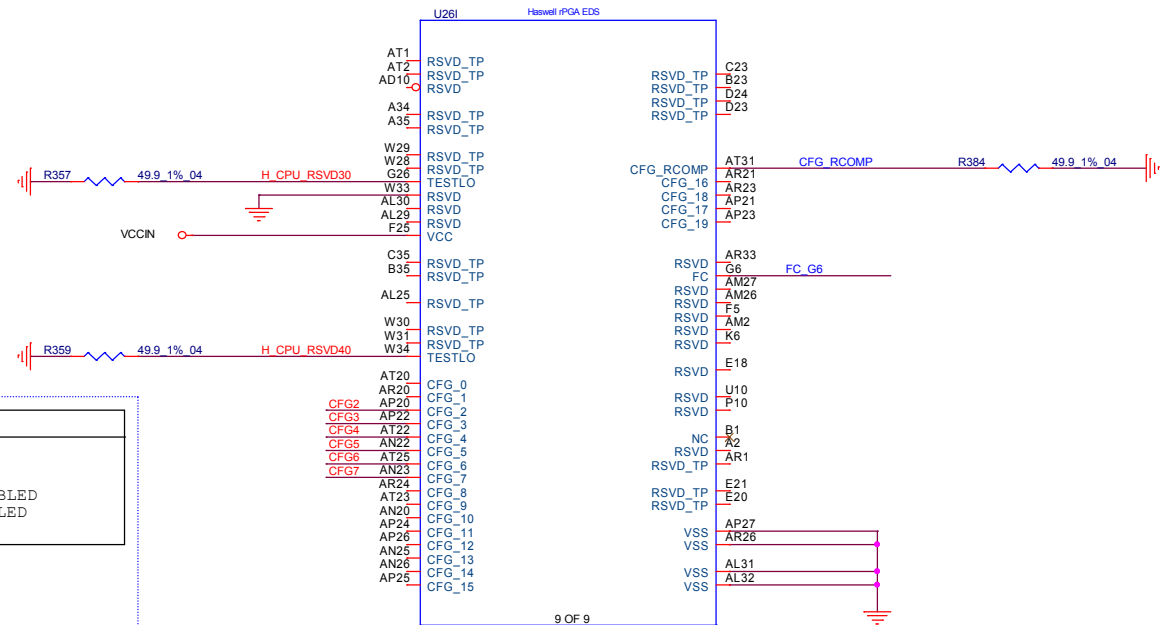
CFG6 R378 \*1K\_04

## DEFENSIVE PULL DOWN SITE

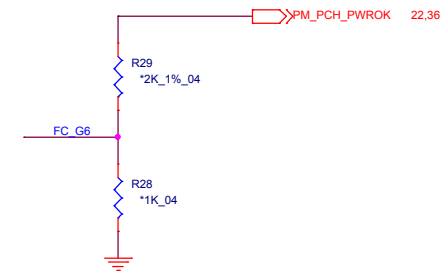
CFG7 R63 \*1K\_04

NOTE:  
PHYSICAL DEBUG ENABLED (DFX PRIVACY)  
0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR  
1 : DISABLED

CFG3 R67 \*1K\_04



NOTE:  
RESERVE THIS CIRCUIT FOR FUTURE COMPATIBILITY



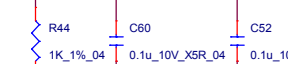
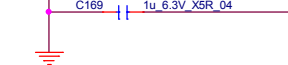
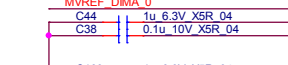
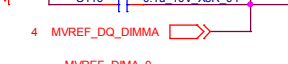
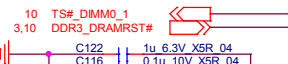
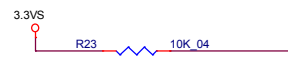
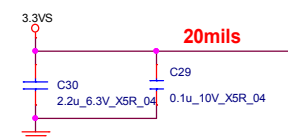
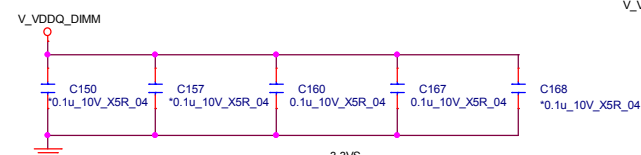
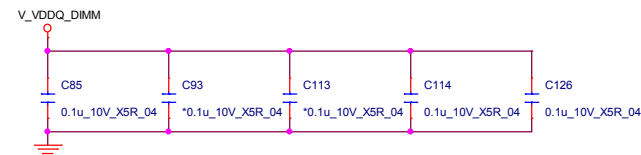
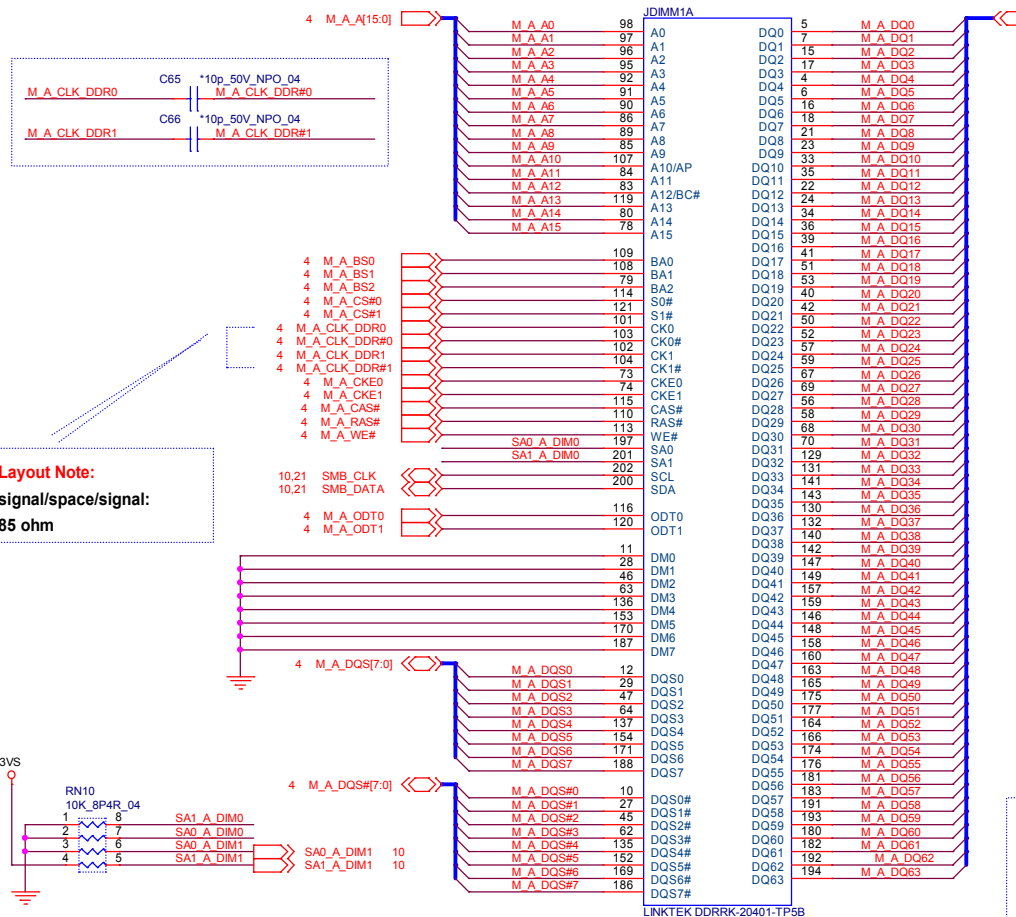
藍天電腦 CLEVO CO.

Title			
[08] PROCESSOR 7/7			
Size	Document Number	Rev	
Custom	6-7P-W65J4-001	6-71-W65J0-D01 1.0	
Date:	Wednesday, October 09, 2013	Sheet	8 of 46

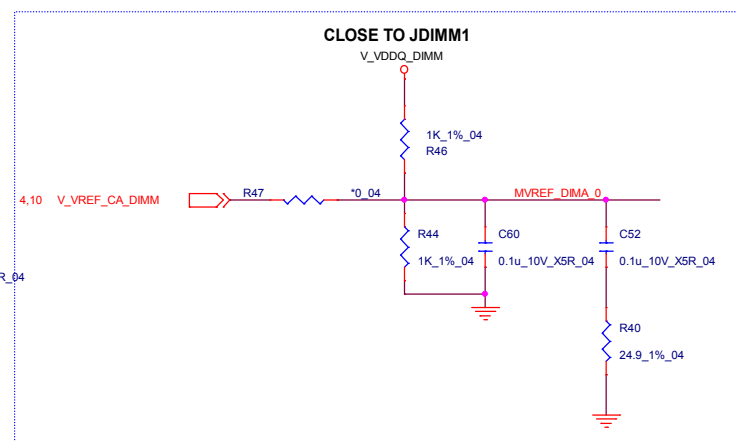
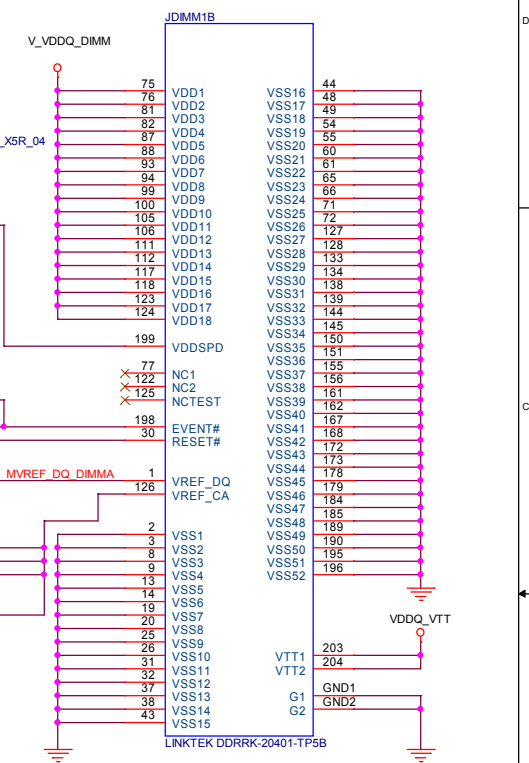
5.41 VCCIN



## CHANGE TO STANDARD



5.2mm  
6-86-24204-005  
6-86-24204-002

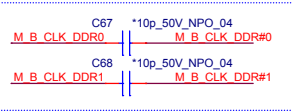


藍 天 電 腦 CLEVO CO.

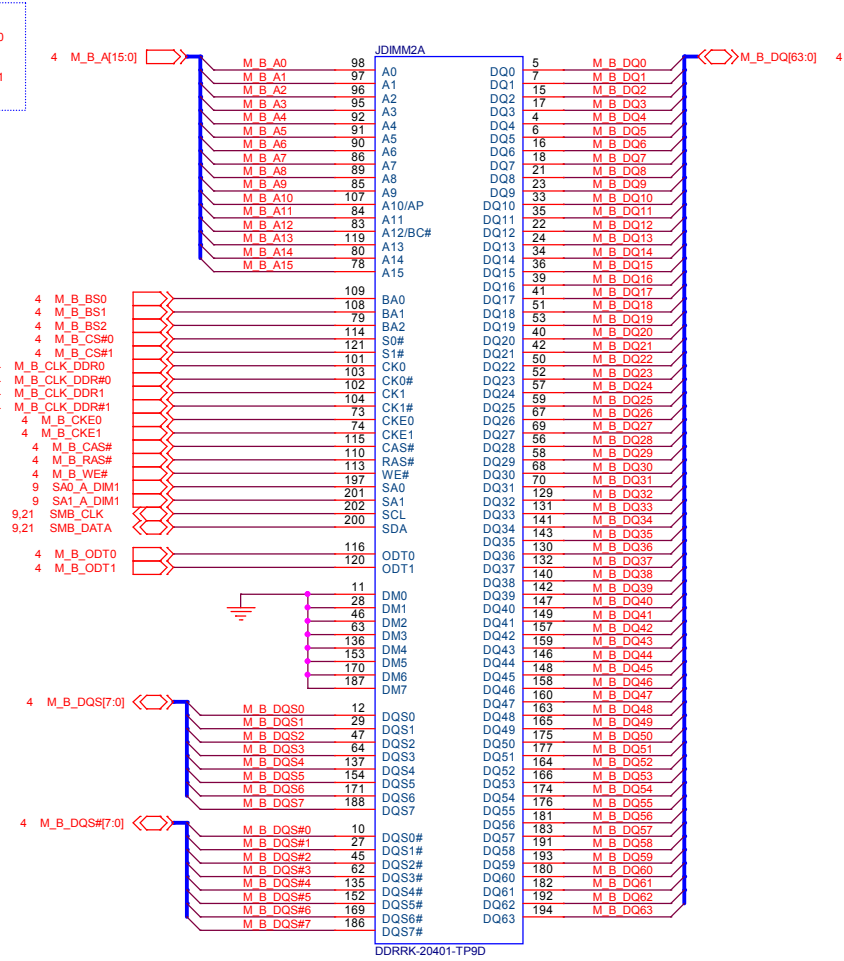
SO-DIMM B\_0

CHANGE TO STANDARD

9.2mm  
6-86-24204-001  
6-86-24204-006



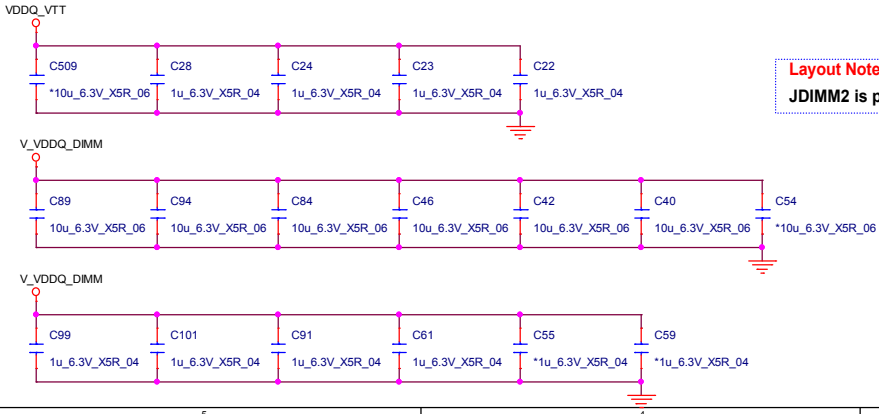
Layout Note:  
signal/space/signal:  
8 / 4 / 8



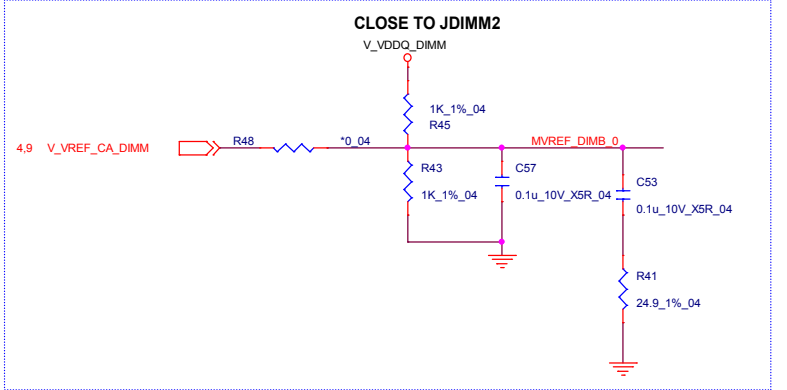
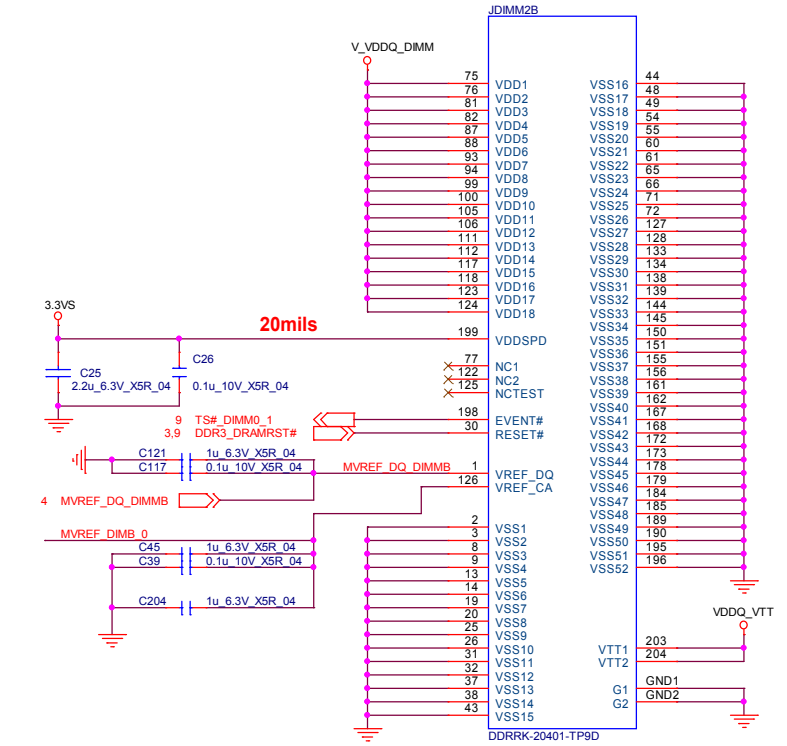
- 4 M\_B\_BS0
- 4 M\_B\_BS1
- 4 M\_B\_BS2
- 4 M\_B\_CS#0
- 4 M\_B\_CS#1
- 4 M\_B\_CLK\_DDR0
- 4 M\_B\_CLK\_DDR1
- 4 M\_B\_CKE0
- 4 M\_B\_CKE1
- 4 M\_B\_CAS#
- 4 M\_B\_RAS#
- 4 M\_B\_WE#
- 9 SA0\_A\_DIM1
- 9 SA1\_A\_DIM1
- 9,21 SMB\_CLK
- 9,21 SMB\_DATA
- 4 M\_B\_ODT0
- 4 M\_B\_ODT1

- 4 M\_B\_DQS[7:0]
- 4 M\_B\_DQS#7[0]

- 4 M\_B\_DQS#0
- 4 M\_B\_DQS#1
- 4 M\_B\_DQS#2
- 4 M\_B\_DQS#3
- 4 M\_B\_DQS#4
- 4 M\_B\_DQS#5
- 4 M\_B\_DQS#6
- 4 M\_B\_DQS#7

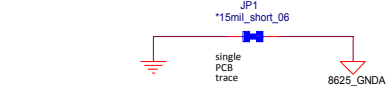


Layout Note:  
JDIMM2 is placed farther from the GMCH than JDIMM1

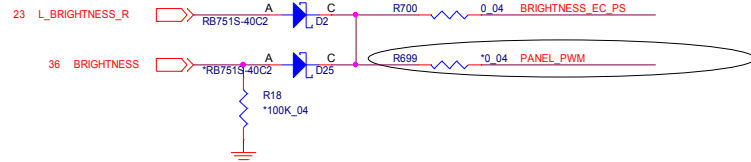
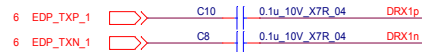
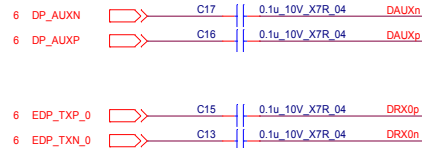


藍天電腦 CLEVO CO.			
[10]DDR3 SO-DIMM_B_0			
Size A3	Document Number 6-7P-W65J4-001	6-71-W65J0-D01	
Date: Wednesday, October 09, 2013	Sheet 10	of 46	Rev 1.0

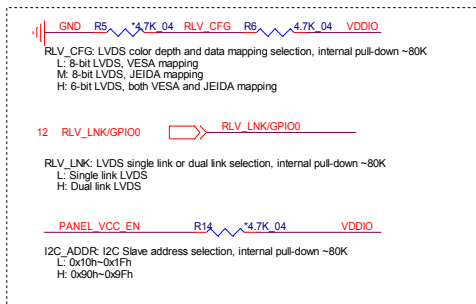
1. Place the switching regulator inductor (L3) close to SW\_OUT Pins (Pin15, Pin16).
2. The SW\_OUT output traces should be as wide as possible.
3. The GND pins (Pin17, Pin18) should be connected to the main PCB ground plane, with the device GND pins of the PS8625 connected to separate GND island (GNDa) for the device. The GND island (GNDa) should be connected to the main GND plane (GND) with a single-point connection by use of a wide PCB trace.
4. Place the 4.7uF decoupling Capacitor (C4) for VDDIOX close to VDDIOX pin.
5. The GND of the 4.7uF capacitor (C4) for VDDIOX should be placed close to the GND of 4.7uF capacitor (C5) behind Inductor.
6. Place the bead (L2) for VDDIOX close to PS8625.



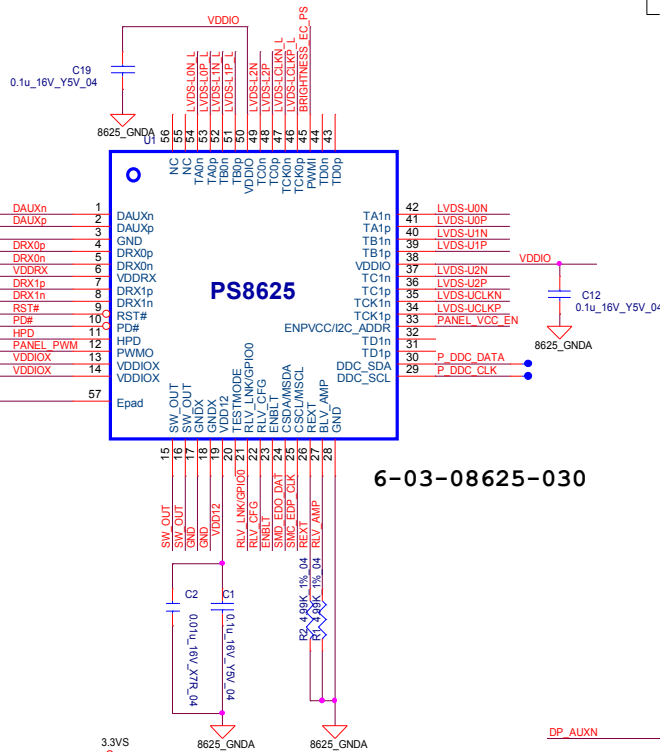
6.12 EDP\_HPD << R9 1K\_04 HPD



### Power On Configuration

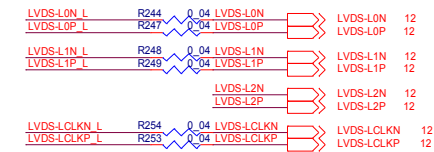


36 SMC\_EDP\_CLK  
36 SMD\_EDO\_DAT

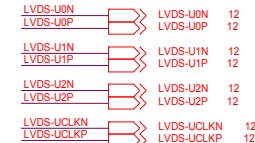


6-03-08625-030

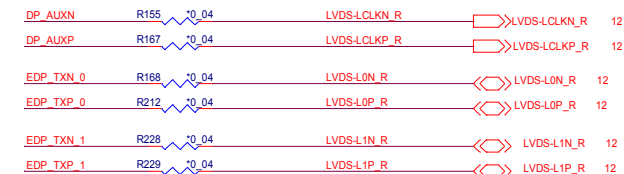
Single link  
LVDS



Dual link  
LVDS



To LVDS Connector

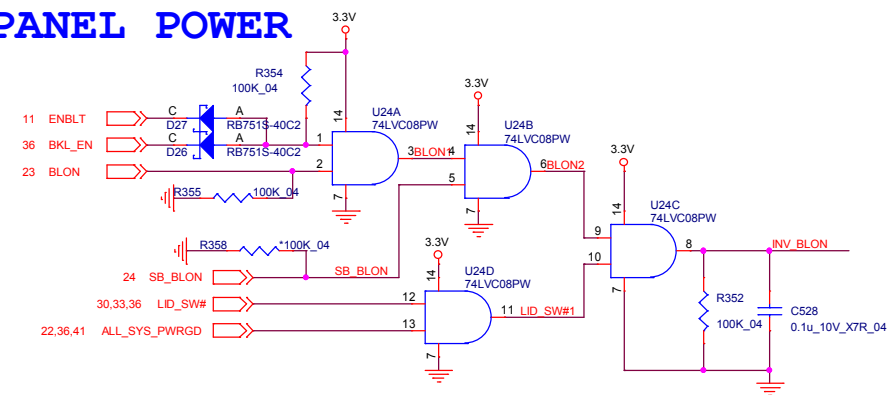
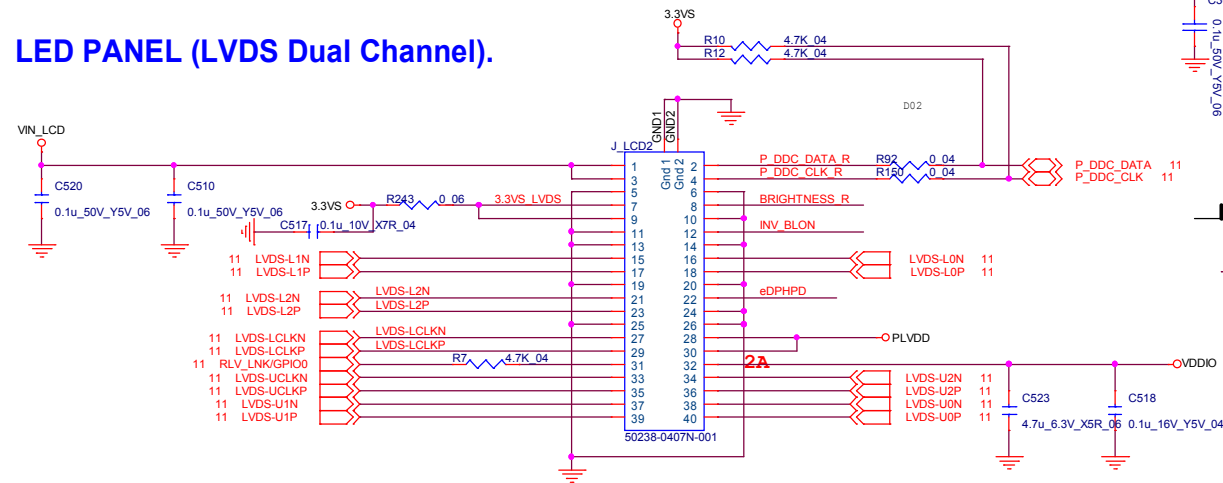


12 VDDIO  
3.3VS

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Title [11] PS8625(EDP TO LVDS)			
Size Custom	Document Number 6-7P-W65J4-001	6-71-W65J0-D01	Rev 1.0
Date: Wednesday, October 09, 2013	Sheet 11	of 46	

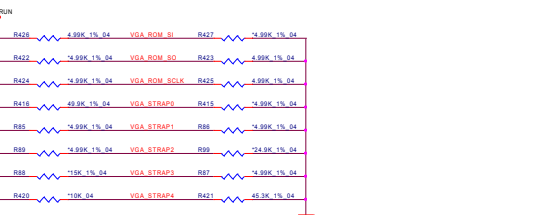
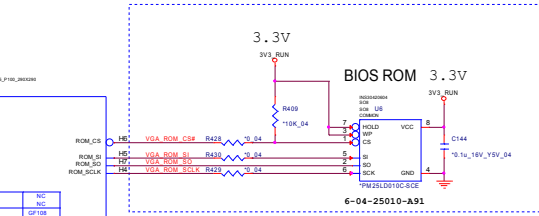
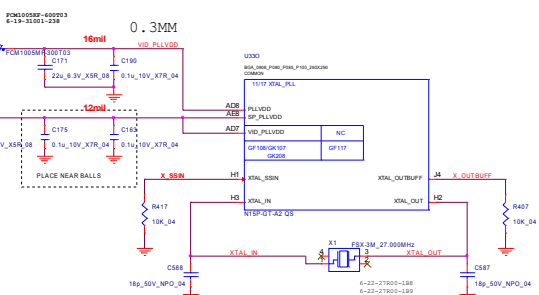
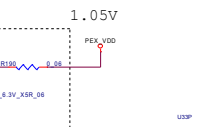
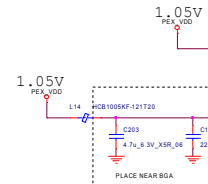
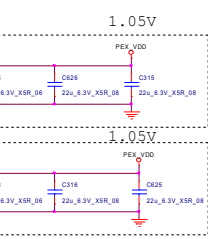
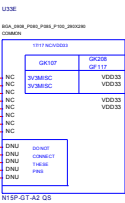
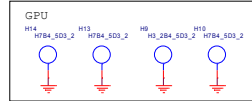
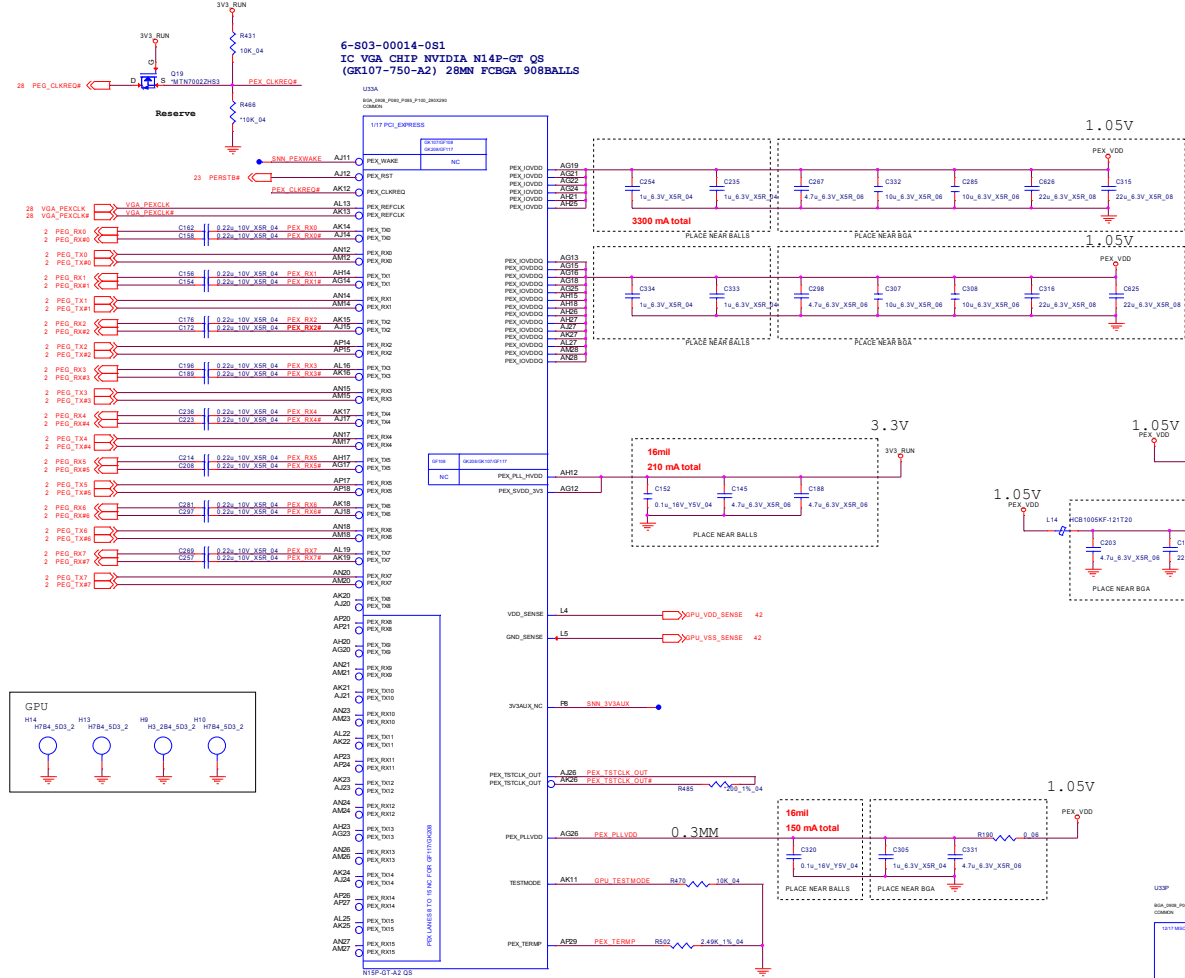
3.6,9,10,12,19,20,21,22,23,24,26,27,28,29,30,31,32,33,34,35,36,37,41

## BRIGHTNESS

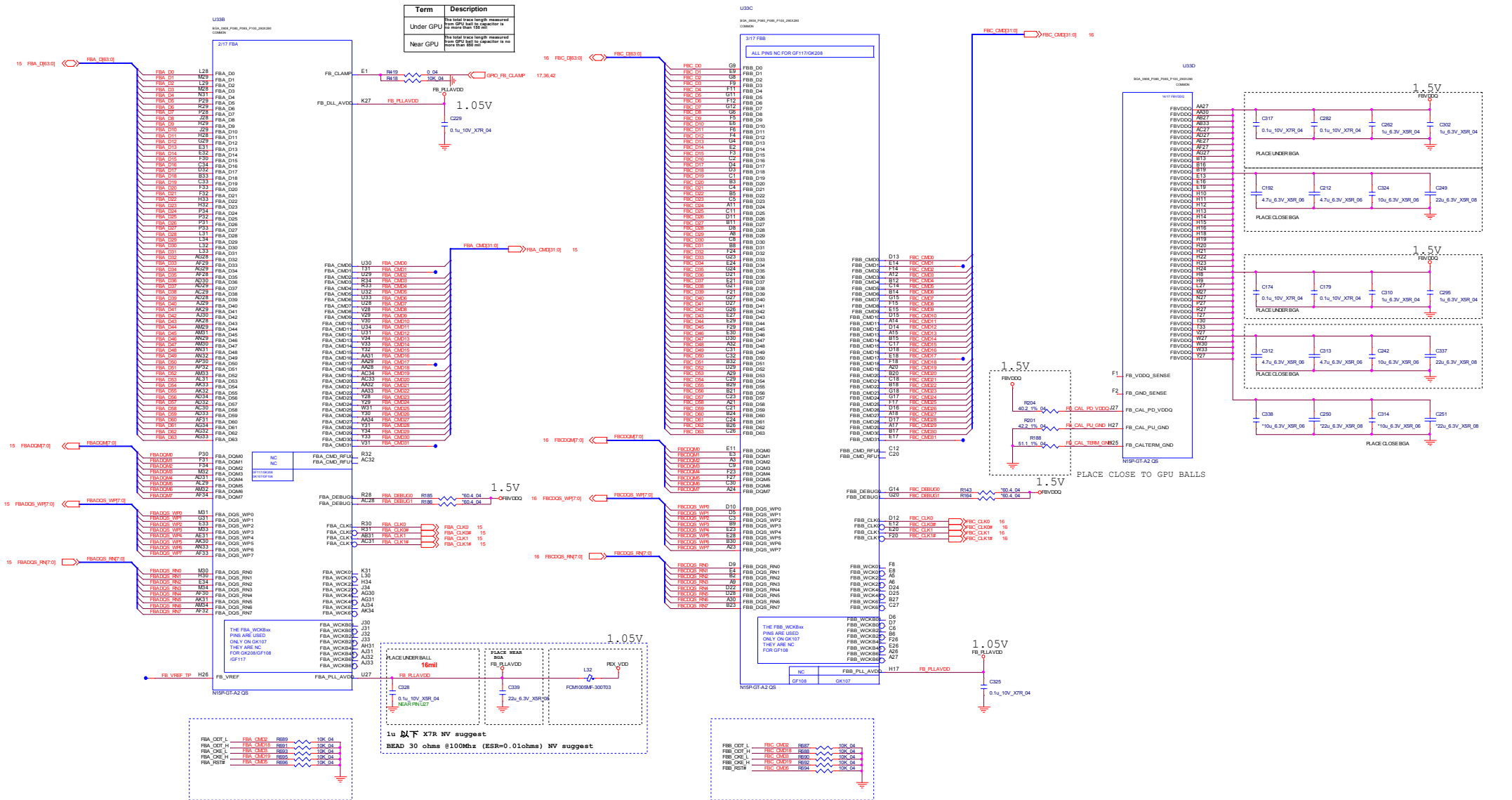
Rev  
1.0

11 VDDIO  
37,38,39,42 SYS15V  
37,38,39,40,41,42,43 VIN  
19,20,30,33,34,35,37,41,42 5VS  
2,3,17,20,24,25,28,29,31,33,35,37,38,40,42 3.3V  
3,6,9,10,11,19,20,21,22,23,24,26,27,28,29,30,31,32,33,34,35,36,37,41 3.3VS

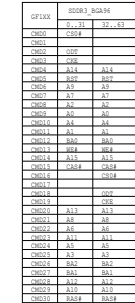
6-803-00014-081  
IC VGA CHIP NVIDIA N14P-GT QS  
(GK107-750-A2) 28MN FCBGA 908BALLS



## Frame Buffer Interface

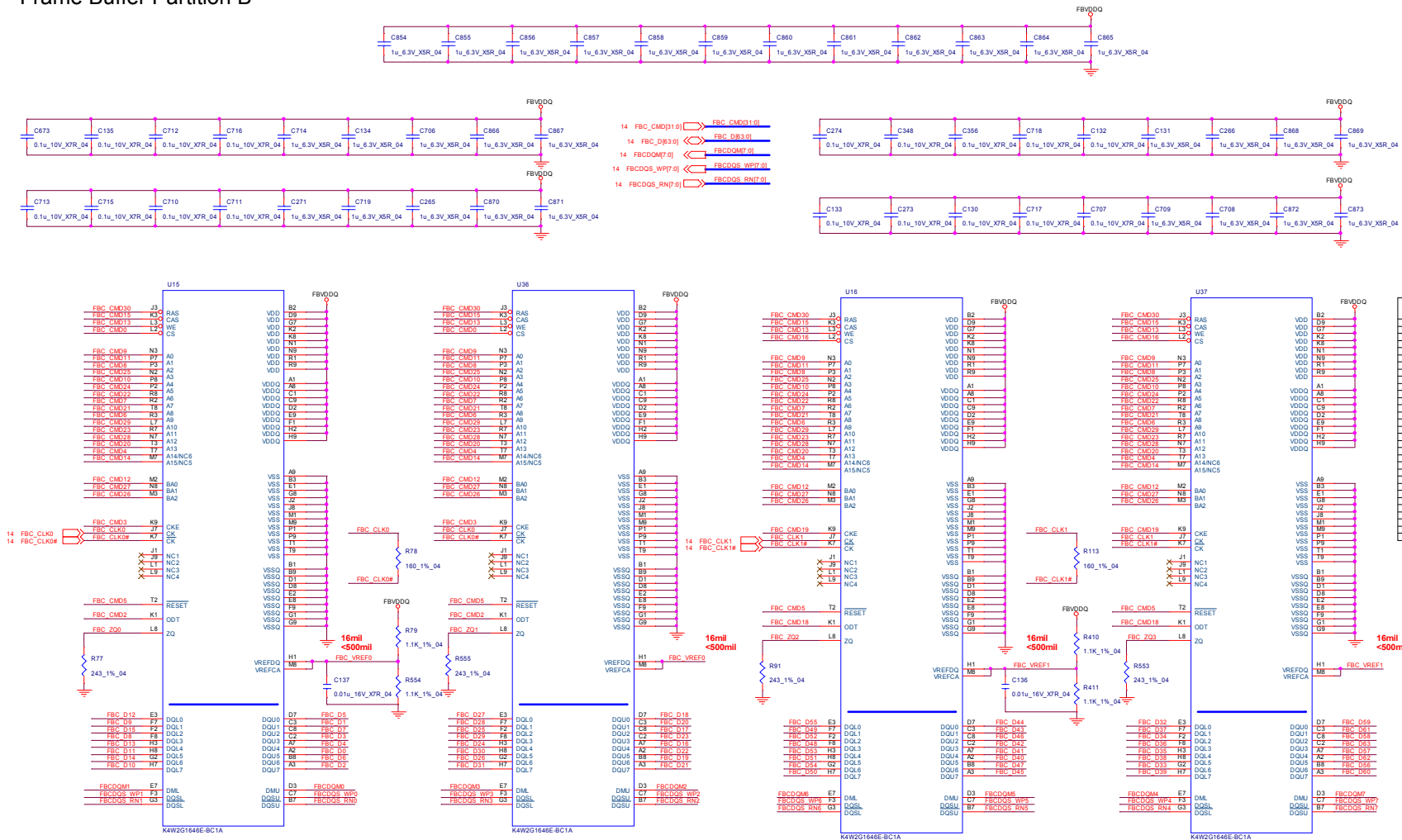


0.1uF X4 for FBVDDQ one chip VRAM  
1.0uF X8



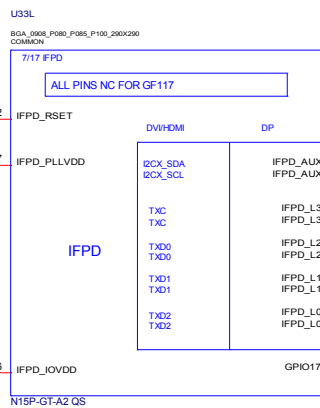


### Frame Buffer Partition B



GFIXX	SDGR3_BGA36	
	6, 31	22, 63
CN00	C00	C00
CN02	C02	C02
CN03	C03	C03
CN04	A14	A14
CN05	A3	A3
CN06	A7	A7
CN07	S2	S2
CN08	A6	A6
CN10	A4	A4
CN11	B1	B1
CN12	S40	S40
CN13	S45	S45
CN15	A15	A15
CN16	S348	S348
CN17	C07	C07
CN18	C08	C08
CN20	A13	A13
CN21	A8	A8
CN22	A5	A5
CN23	A11	A11
CN24	A5	A5
CN25	A3	A3
CN26	S43	S43
CN27	S41	S41
CN28	A12	A12
CN29	A14	A14





The diagram illustrates the pin configuration for the U33M module, showing connections for two main functional blocks: IFPE and IFPF. The module is connected to a system bus (U33M) and various peripheral components.

**U33M Pin Connections:**

- AB8:** IFPE\_PLLVDD
- AD6:** IFPE\_F\_RSET
- AC7:** IFPE\_I\_OVDD
- AC8:** IFPF\_I\_OVDD

**IFPE Block Connections:**

- 8/17 IFPEF:** ALL PINS NC FOR GF117
- IFPE:**
  - IFPE\_AUX:** IFPE\_AUX1, IFPE\_AUX2
  - IFPE\_L3:** IFPE\_L31, IFPE\_L32
  - IFPE\_L2:** IFPE\_L21, IFPE\_L22
  - IFPE\_L1:** IFPE\_L11, IFPE\_L12
  - IFPE\_L0:** IFPE\_L01, IFPE\_L02

**IFPF Block Connections:**

- IFPF:**
  - IFPF\_AUX:** IFPF\_AUX1, IFPF\_AUX2
  - IFPF\_L3:** IFPF\_L31, IFPF\_L32
  - IFPF\_L2:** IFPF\_L21, IFPF\_L22
  - IFPF\_L1:** IFPF\_L11, IFPF\_L12
  - IFPF\_L0:** IFPF\_L01, IFPF\_L02

**Peripheral Connections:**

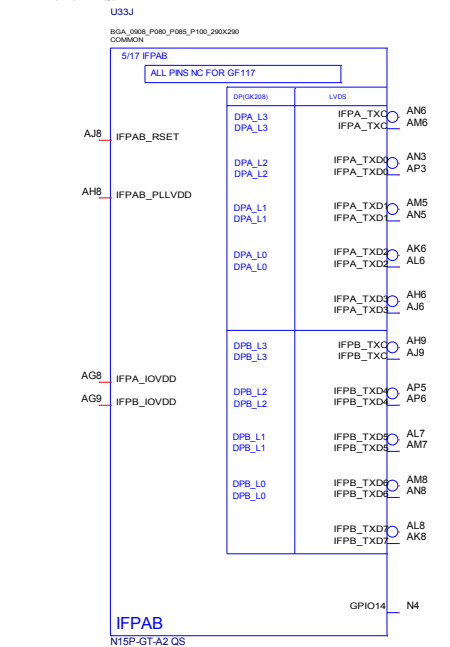
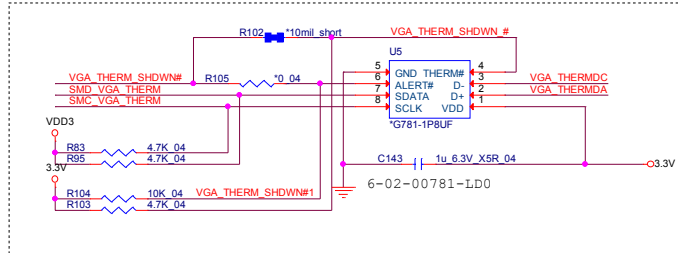
- DVI-DL:** I2CY\_SDA, I2CY\_SCL
- DVI-SL/HDMI:** I2CY\_SDA, I2CY\_SCL
- DP:** NC FOR GK208
- GPIO18:** HPD\_E
- GPIO19:** HPD\_F

**Other Connections:**

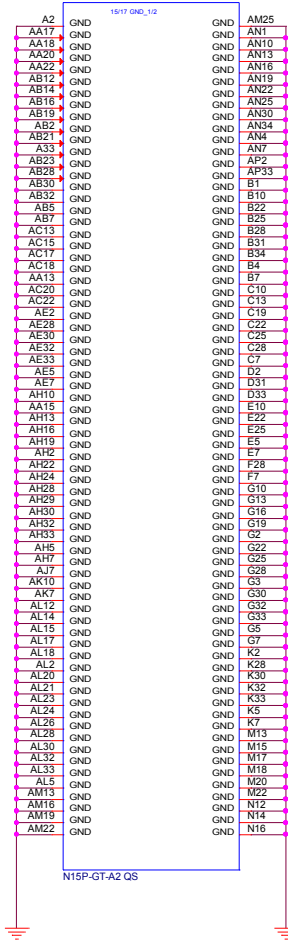
- NC FOR GK208:** Multiple connections for NC FOR GK208 are shown across the diagram.

**Legend:**

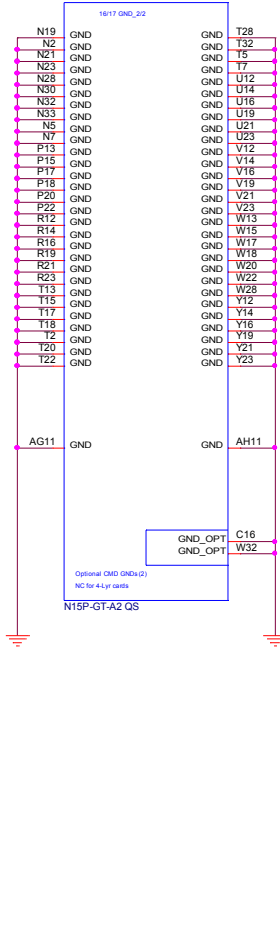
- U33M:** BGA\_9088\_P080\_P085\_P100\_20x20x20 COMMON
- U33M:** N15P-GT-A2 QS



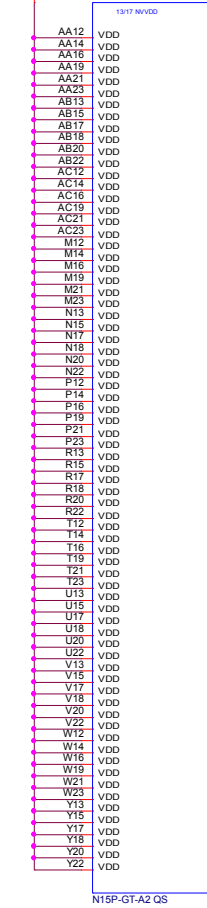
## U33F

BGA\_0908\_P080\_P085\_P100\_200x290  
COMMON

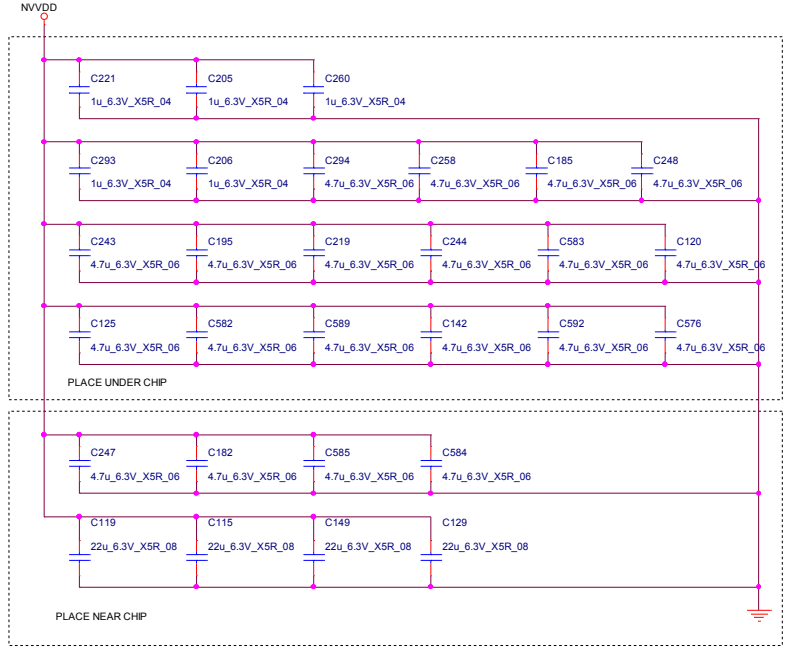
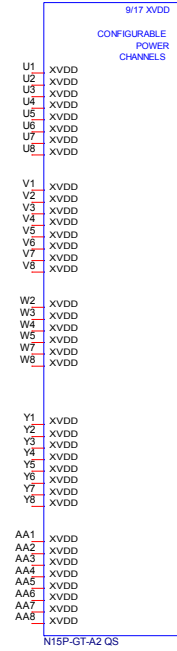
## U33G

BGA\_0908\_P080\_P085\_P100\_200x290  
COMMON

## U33H

BGA\_0908\_P080\_P085\_P100\_200x290  
COMMON

## U33I

BGA\_0908\_P080\_P085\_P100\_200x290  
COMMON

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Title [18] VGA NVDD Decoupling

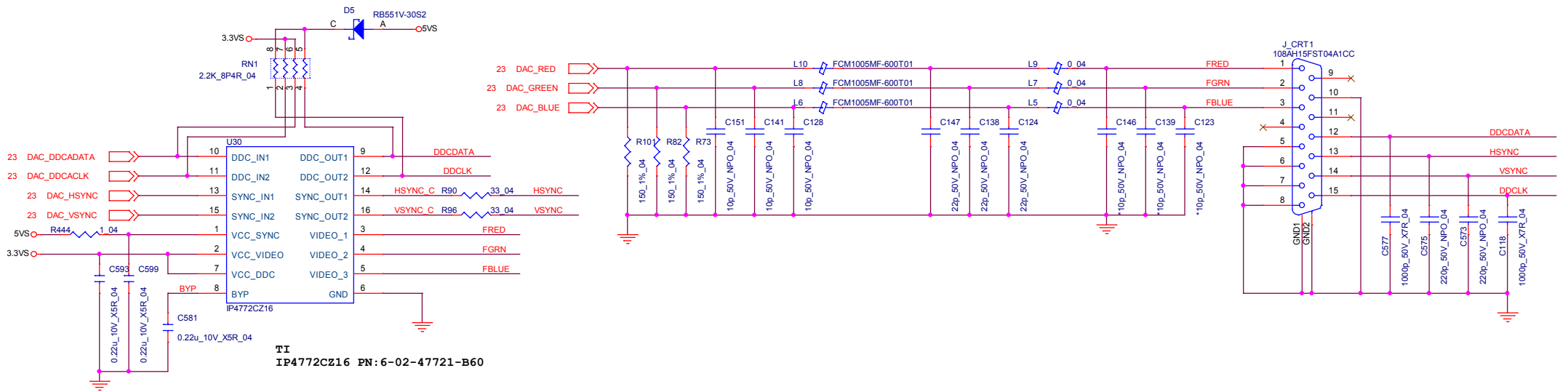
Size Document Number 6-71-W6500-D03 Rev 3.0

Date: Wednesday, October 09, 2013 Sheet 18 of 46

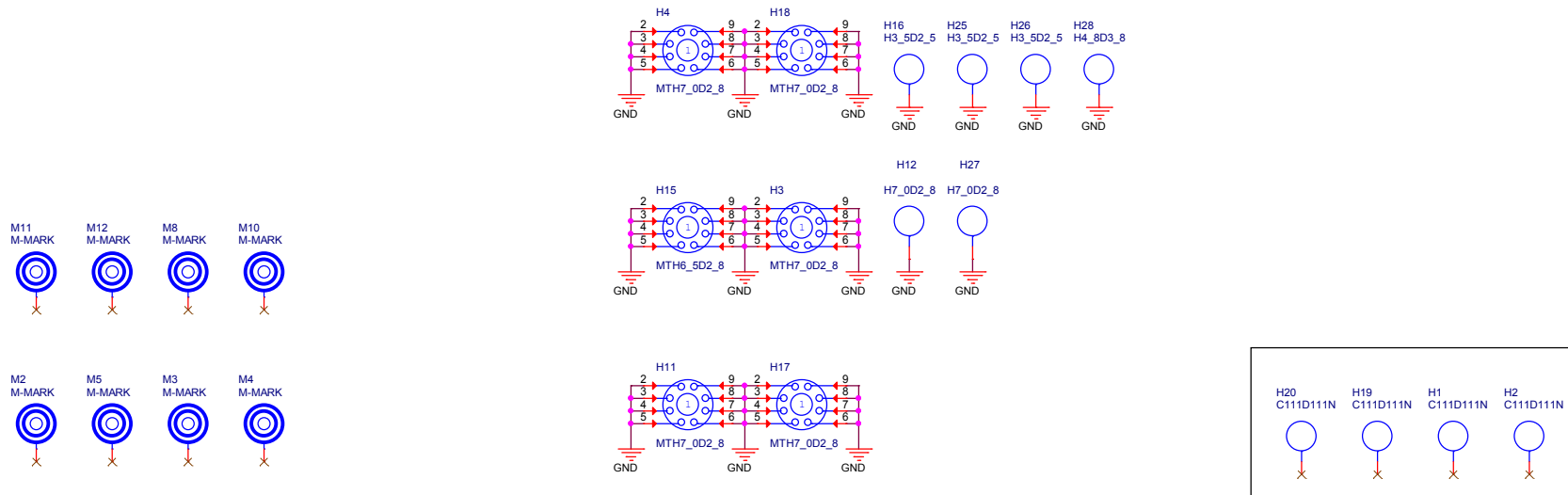
17,20,21,22,24,26,27,28,29,30,32,33,36,37,38,39,43

VDD3  
NVDD  
3V3\_RUN

## CRT



## M/B PCH



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[19]CRT

Size A3	Document Number 6-7P-W65J4-001	6-71-W65J0-D01	Rev 1.0
Date:	Wednesday, October 09, 2013	Sheet	19 of 46

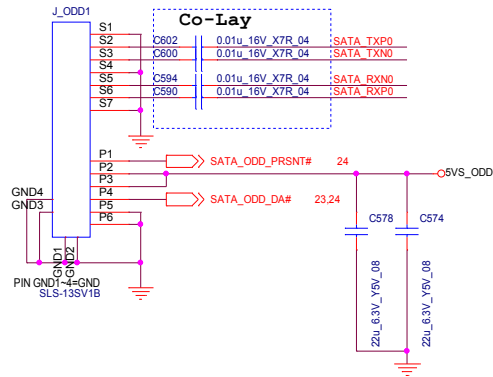
3,6,9,10,11,12,20,21,22,23,24,26,27,28,29,30,31,32,33,34,35,36,37,41  
12,20,30,33,34,35,37,41,42

3.3VS  
5VS

# Lynx Point - M (HDA, JTAG, SATA)

## ODD CONN

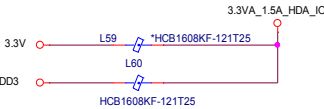
W650SR



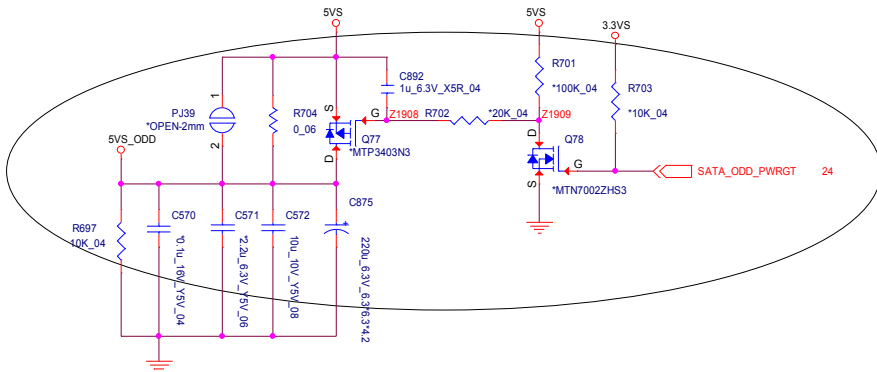
JOPEN1	CLEAR COMS
JOPEN2	CLEAR ME RTC REGISTER

Flash Descriptor  
Security Override  
Low = Disabled-(Default)  
High = Enabled

INTVPMEN - INTEGRATED SUS 1.05V VRM ENABLE  
HIGH - ENABLE INTERNAL VR'S  
LOW - ENABLE EXTERNAL VR'S



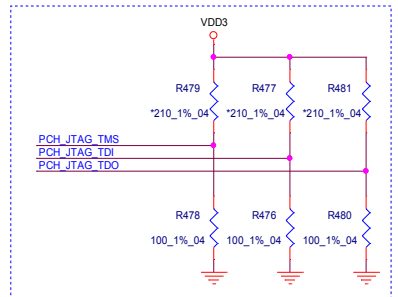
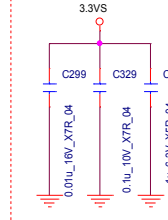
## ODD Zero Power ODD



27 3.3VA\_1.5A\_HDA\_IO  
22.27 RTCVCC  
22.26, 27, 28, 40, 42 1.5VS  
12.19, 30, 33, 34, 35, 37, 41, 42 5VS  
17.21, 22, 24, 26, 27, 28, 29, 30, 32, 33, 36, 37, 38, 39, 43 VDD3  
2.3, 12, 17, 24, 25, 28, 29, 31, 33, 35, 37, 38, 40, 42 3.3V  
3.6, 9, 10, 11, 12, 19, 21, 22, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 41 3.3VS

## Layout Note:

Closed to U4



## 藍天電腦 CLEVO CO.

[20] Lynx 1/9-RTC/HDA/SATA

Size	Document Number	Rev
Custom	6-71-W65J0-D01	1.0

Date: Wednesday, October 09, 2013 Sheet 20 of 46

## SATA ODD

BC8	SATA_RXN0
BE8	SATA_RXP0
AW8	SATA_TXN0
AY8	SATA_TXP0

## E-SATA HDD

BB9	SATARXN2	31
BD9	SATARXP2	31
AY13	SATATXN2	31
AW13	SATATXP2	31

## MSATA HDD

BD13	SATA_RXN4	29
BB13	SATA_RXP4	29
AV15	SATA_TXN4	29
AW15	SATA_TXP4	29

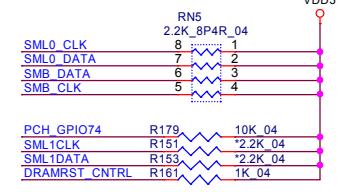
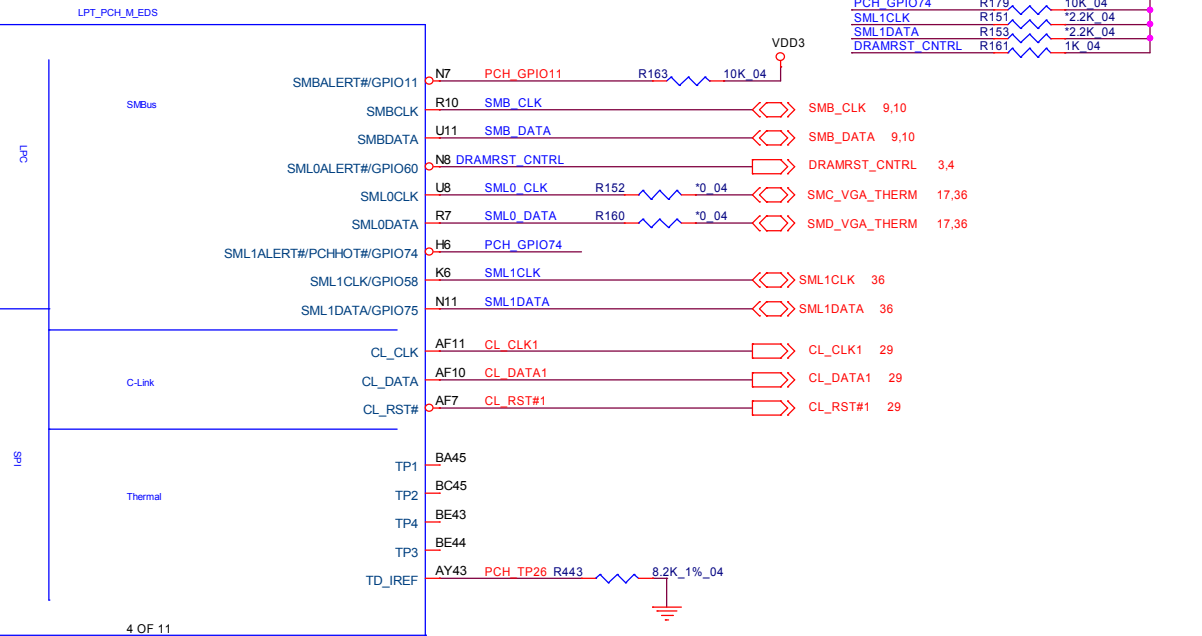
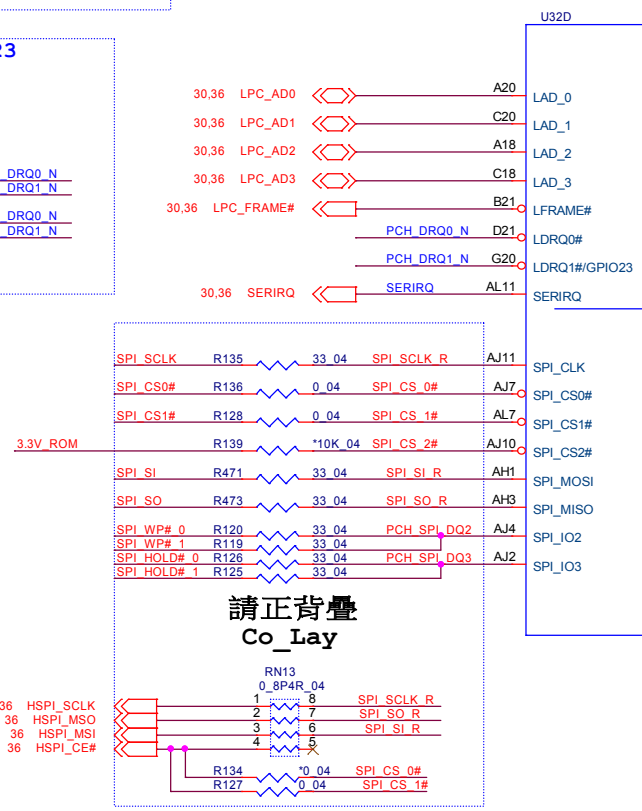
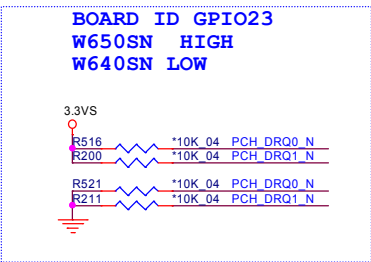
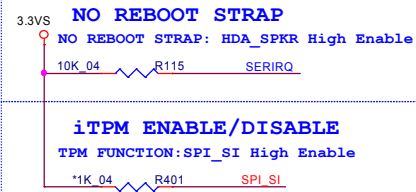
## SATA HDD1

BC14	SATA_RXN5	33
BE14	SATA_RXP5	33
AP15	SATA_TXN5	33
AR15	SATA_TXP5	33

## Boot BIOS Strap

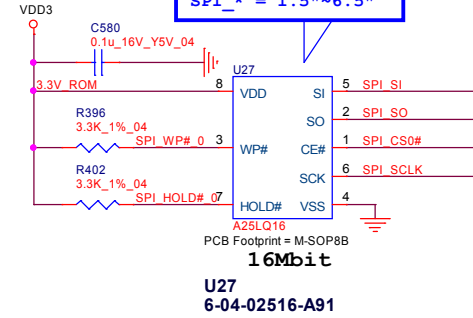
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC (Default)
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

# Lynx Point - M (LPC, SMBUS, SPI, C-LINK)



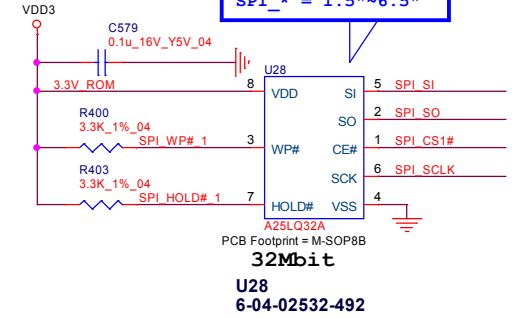
## ME ROM

SPI\_\* = 1.5"~6.5"



## BIOS ROM

SPI\_\* = 1.5"~6.5"

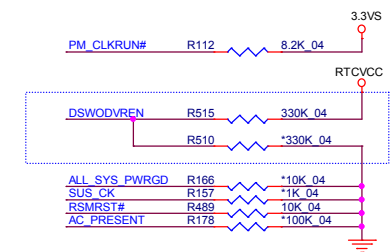
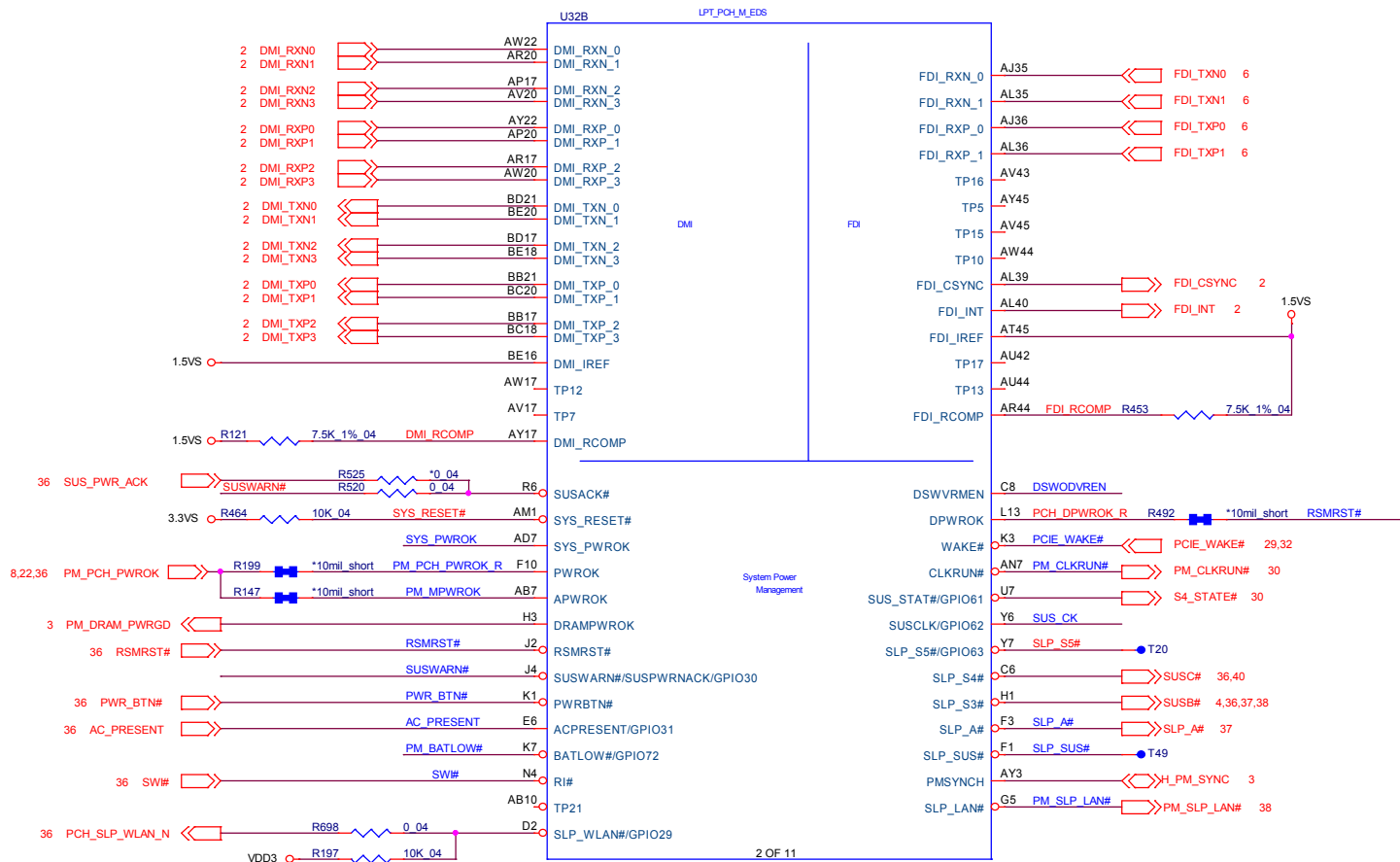


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[21] Lynx 2/9-LPC/SPI/LPC/SMB			
Title	Document Number	6-71-W65J0-D01	
Size	Custom	Rev 1.0	
Date:	Wednesday, October 09, 2013	Sheet	21 of 46

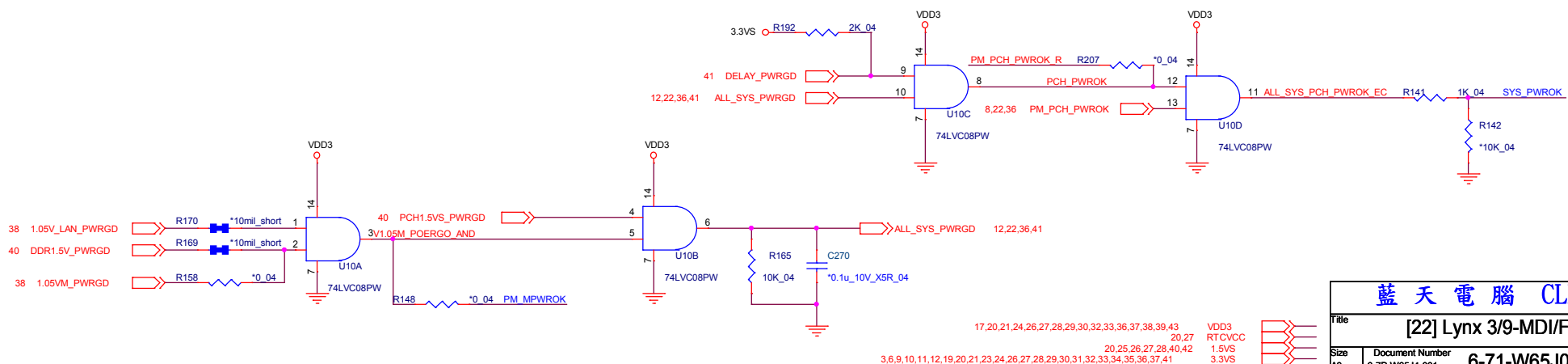
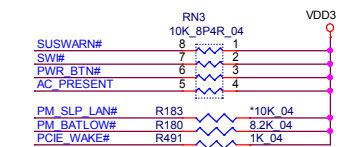
17,20,22,24,26,27,28,29,30,32,33,36,37,38,39,43  
3,6,9,10,11,12,19,20,22,23,24,26,27,28,29,30,31,32,33,34,35,36,37,41

VDD3  
3.3VS

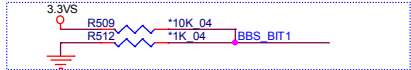
Lynx Point -M (DMI,FDI,PWRGD)



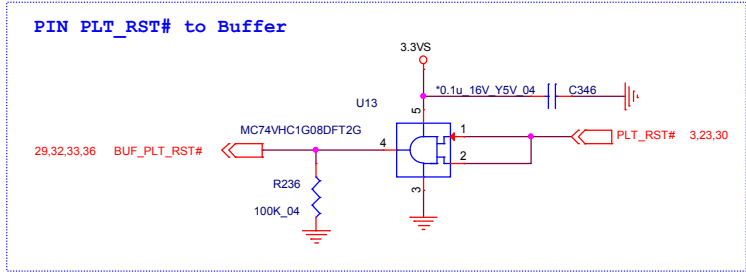
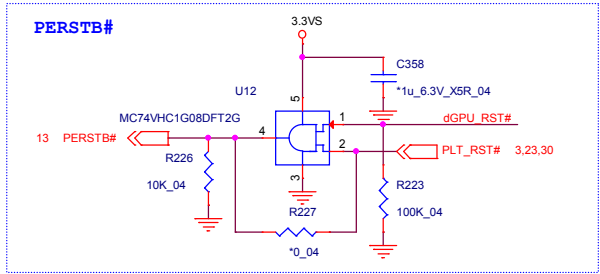
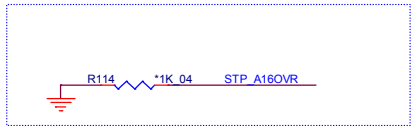
DSWODVREN - ON DIE DSW VR ENABLE	
R426	Enabled (DEFAULT)
R427	Disabled



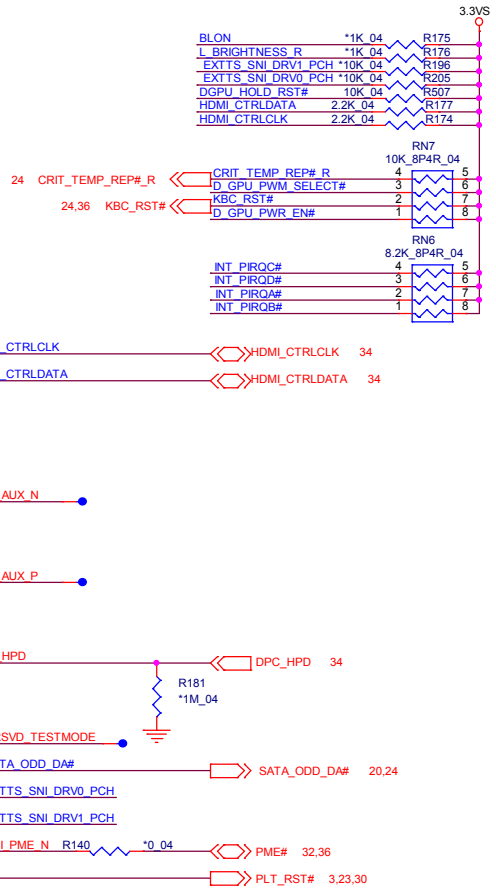
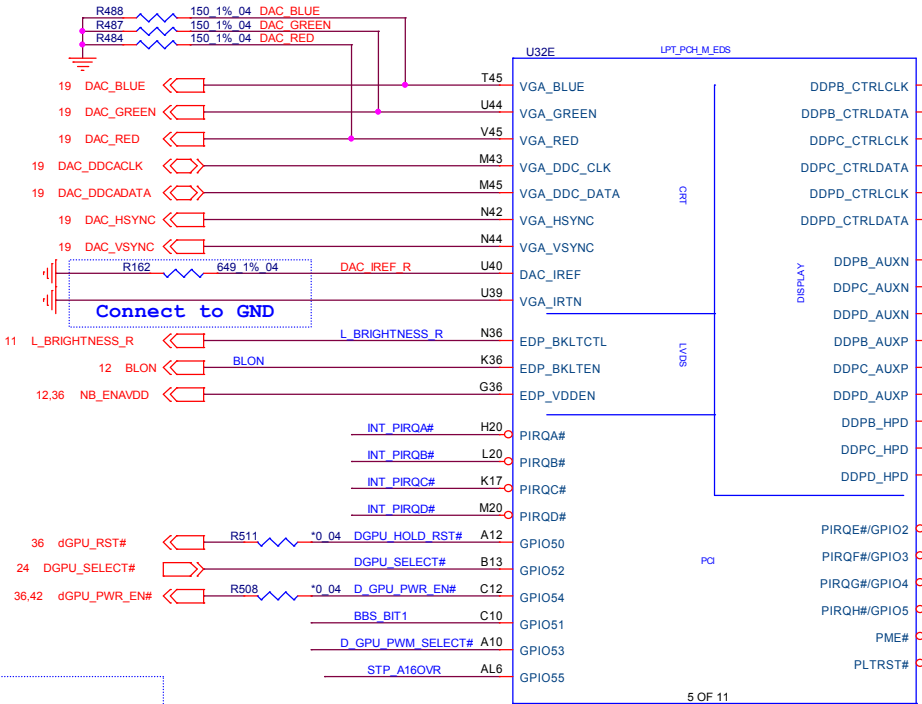
Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



A16 SWAP OVERRIDE STRAP	
STP_A16OVR	LOW = A16 SWAP OVERRIDE HIGH = DEFAULT



## Lynx Point -M (CRT,LVDS,PCI,DISPLAY)



12,19,20,30,33,34,35,37,41,42  
3,6,9,10,11,12,19,20,21,22,24,26,27,28,29,30,31,32,33,34,35,36,37,41

5VS  
3.3VS

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Title

[23] Lynx 4/9-CRT/LVDS/PCI

Size

Document Number

6-71-W65J4-001

Rev

1.0

Date:

Wednesday, October 09, 2013

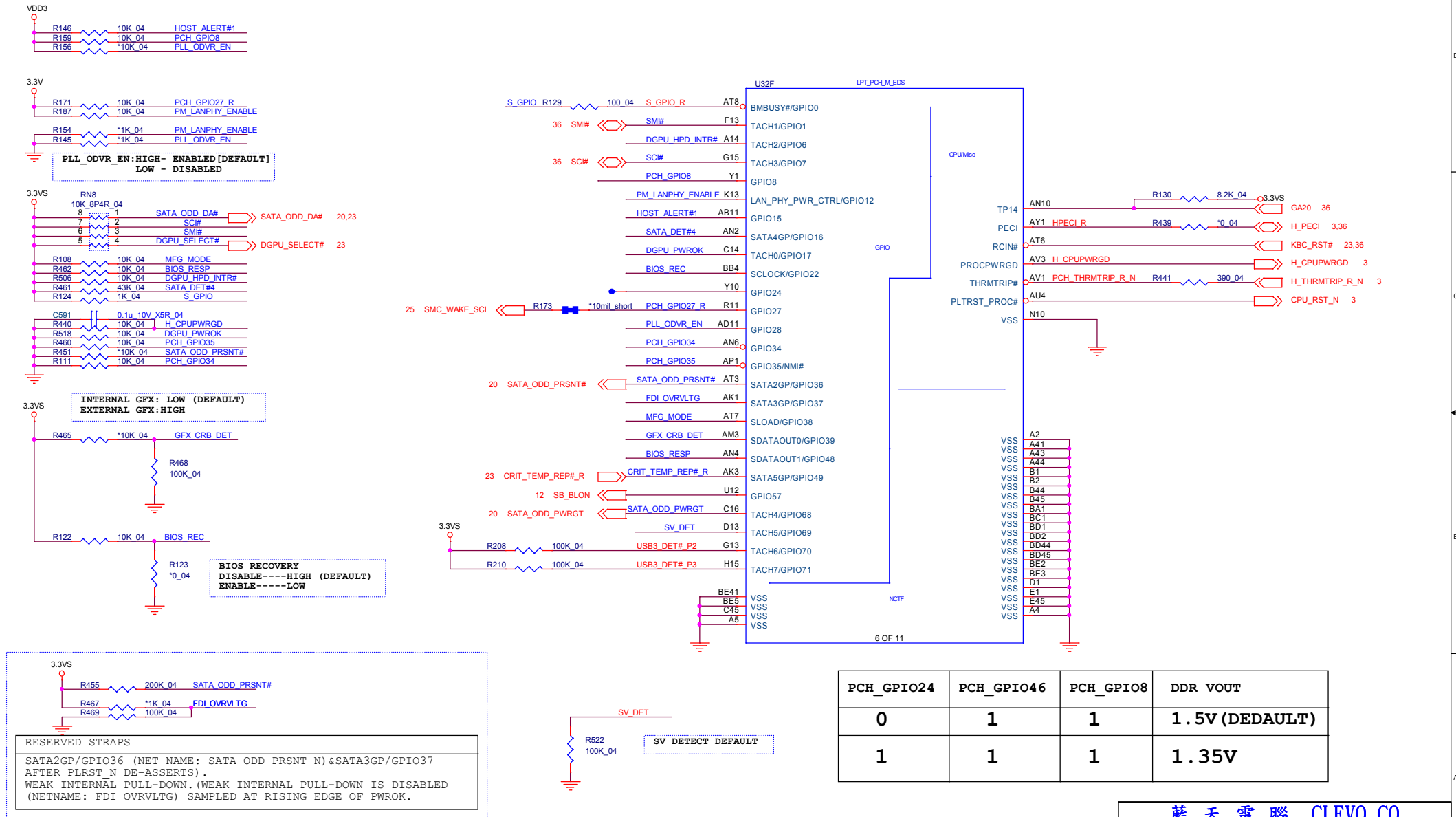
Sheet

23

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46

# Lynx Point - M (GPIO,CPU/MISC,NCTF)



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[24] Lynx 5/9-GPIO/MISC/NCTF

Size	Document Number	6-71-W65J0-D01	Rev
Custom	6-7P-W65J4-001		1.0
Date:	Wednesday, October 09, 2013	Sheet	24 of 46

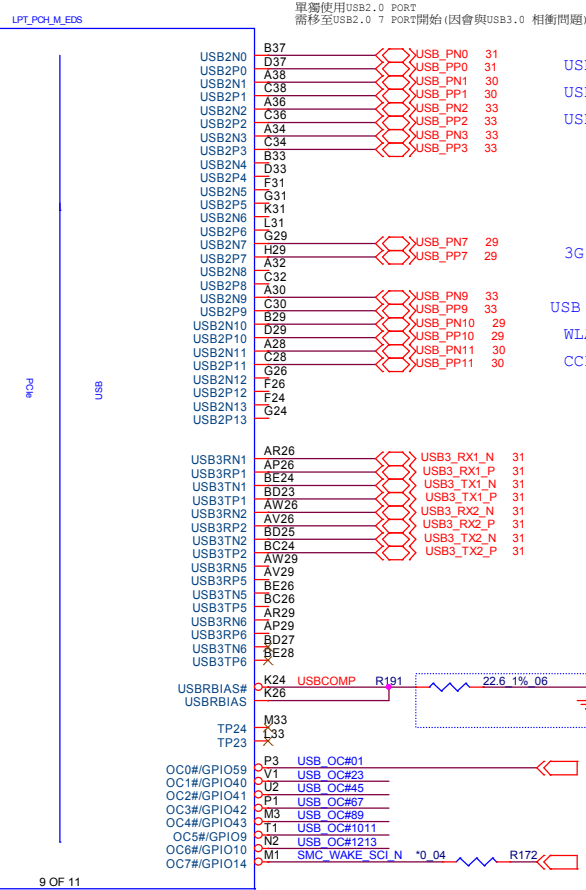
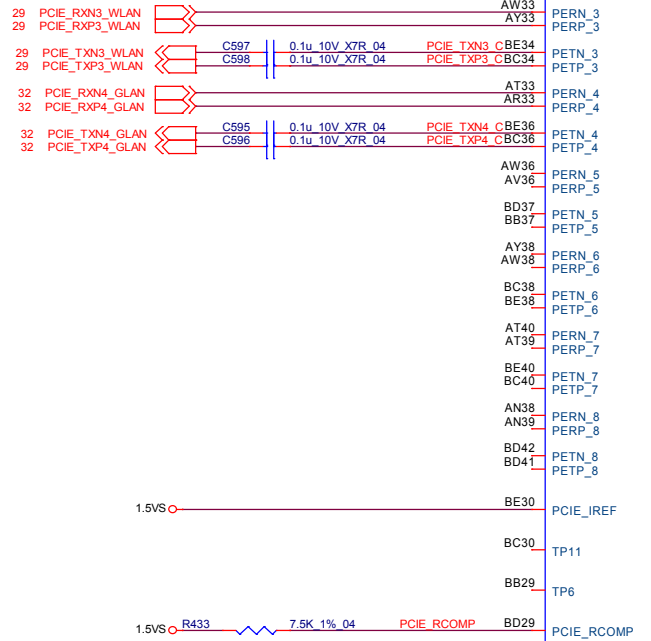
17,20,21,22,26,27,28,29,30,32,33,36,37,38,39,43  
2,3,12,17,20,25,28,29,31,33,35,37,38,40,42  
3,6,9,10,11,12,19,20,21,22,23,26,27,28,29,30,31,32,33,34,35,36,37,41

VDD3  
3.3V  
3.3VS



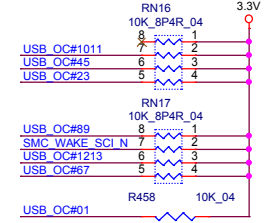
# Lynx Point -M (PCIe,USB)

PCI-E x1	Usage
Lane 1	X
Lane 2	X
Lane 3	WLAN
Lane 4	GLAN / CARD READER
Lane 5	X
Lane 6	X
Lane 7	X
Lane 8	X



USB 3.0 MAPING USB2.0	
USB 3.0 P1	USB 2.0 P0
USB 3.0 P2	USB 2.0 P1
USB 3.0 P3	USB 2.0 P2

USBCOMP (R7F11): TIE TRACES TOGETHER CLOSE TO PINS, WITH LENGTH NO LONGER THAN 450 MILS TO RESISTOR



藍天電腦 CLEVO CO.

Title[25] Lynx 6/9-PCIe/USB

Size6-7P-W65J4-0016-71-W65J0-D01

Custom

DateWednesday, October 09, 2013

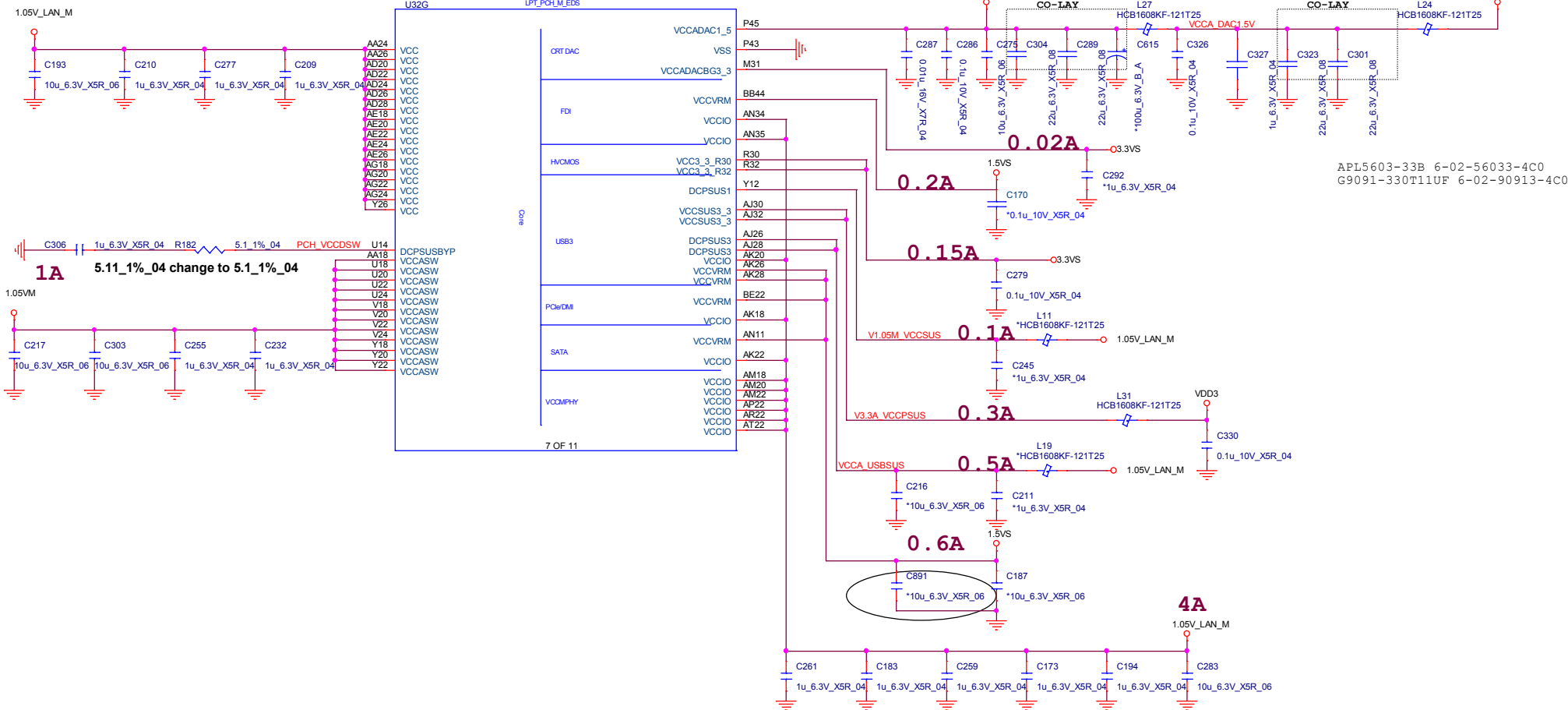
Sheet25

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Rev1.0

20,22,26,27,28,40,42 1.5VS  
17,20,21,22,24,26,27,28,29,30,32,33,36,37,38,39,43 VDD3  
2,3,12,17,20,24,28,29,31,33,35,37,38,40,42 3.3V

1.5A



APL5603-33B 6-02-56033-4C0  
G9091-330T11UF 6-02-90913-4C0

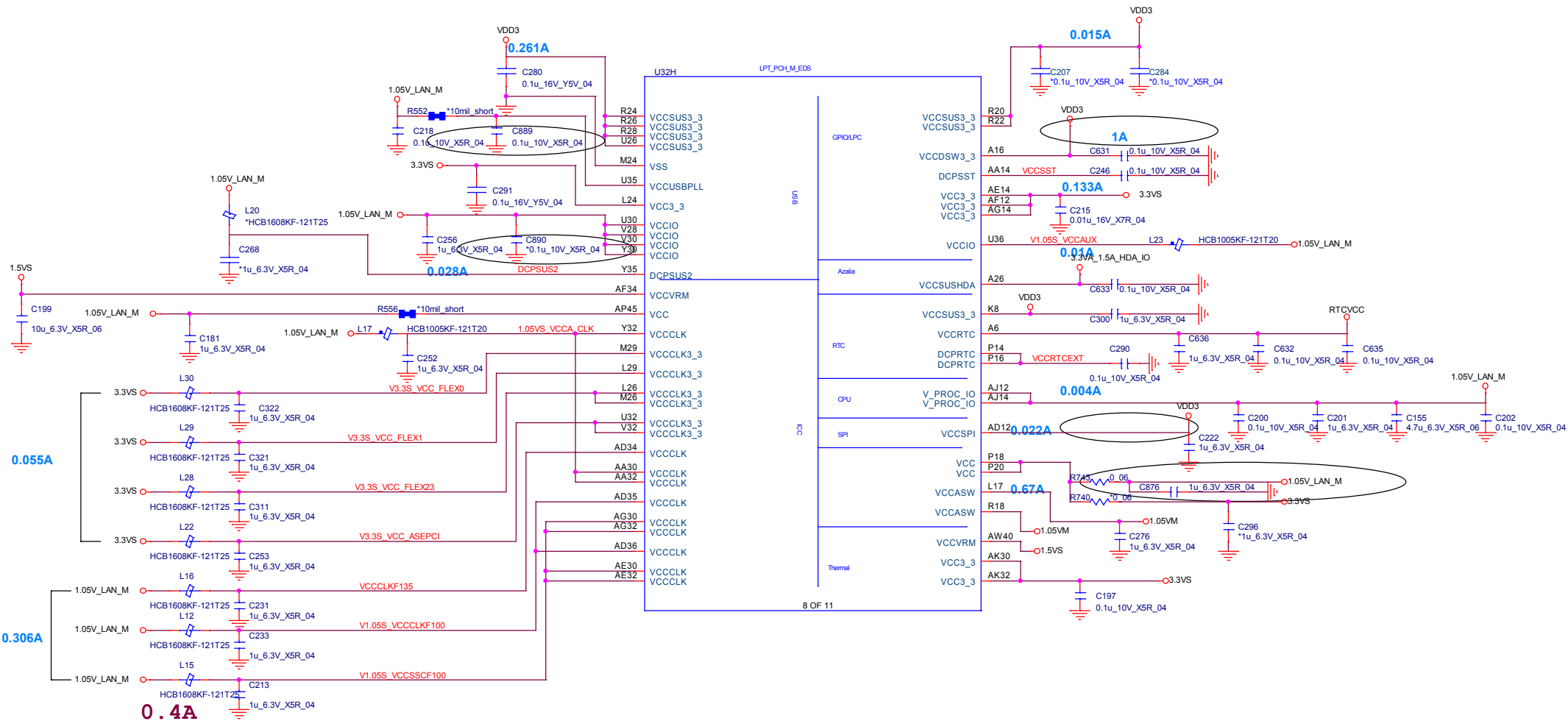
藍天電腦 CLEVO CO.

[26] Lynx 7/9-POWER

Size	Document Number	Rev
Custom	6-71-W65J0-D01	1.0
Date:	Wednesday, October 09, 2013	Sheet 26 of 46

[illegible]

## Lynx Point - M (POWER)



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[27] Lynx 8/9-POWER

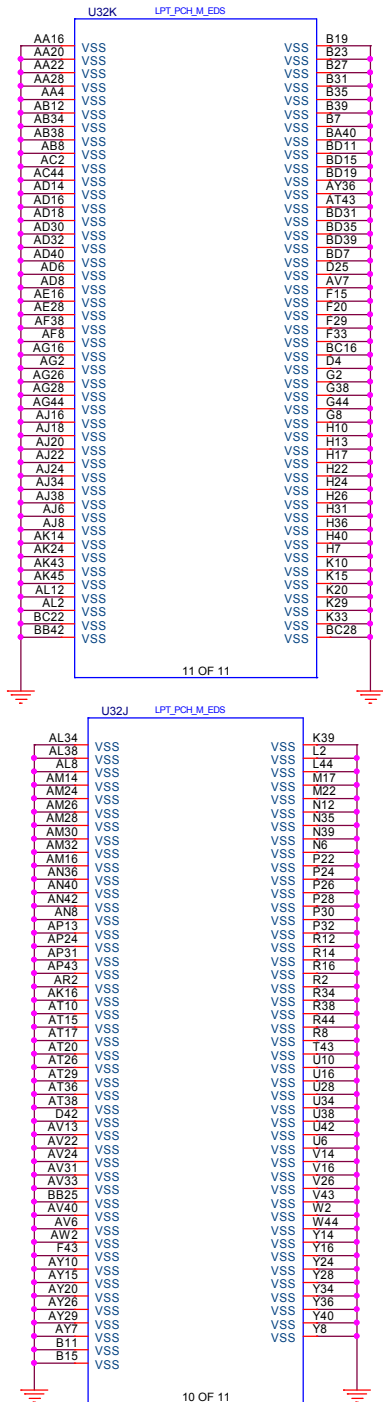
Size	Document Number
A3	6-7P-W65J4-001 6-71-W65J0-D01

Rev	1.0
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Date: Wednesday, October 09, 2013 Sheet 27 of 46

# Lynx Point -M (GND)

# Lynx Point -M (CLK)



100MHz

100MHz

29 CLK\_PCIE\_MIN#  
29 CLK\_PCIE\_MINI  
29 WLAN\_CLKREQ#

32 CLK\_PCIE\_GLAN#  
32 CLK\_PCIE\_GLAN  
28,32 LAN\_CLKREQ#

33 CLK\_PCH\_CARD\_N  
33 CLK\_PCH\_CARD\_P  
33 CARD\_CLKREQ#

PCH\_GPIO46 R482

PCH\_GPIO46 R  
\*10mil\_short  
PCIE CK\_XDP N  
PCIE CK\_XDP P

30 PCLK\_TPM R500

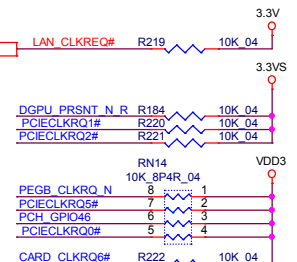
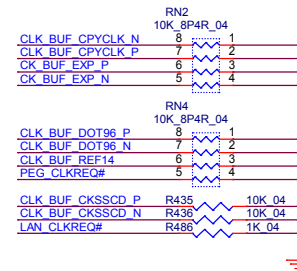
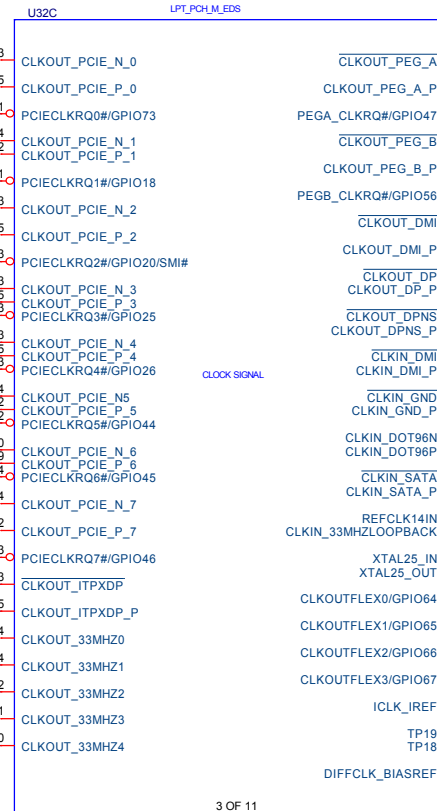
36 PCLK\_KBC R501

CLK\_PCIE\_FB R189

CLK\_PCIE\_KBC R

CLKOUT\_33MHZ0~4  
Breakin 300mils  
Breakout 1500mils

Voltage Rail	Voltage	S0 Iccmax	Current (A)
V_CPU_IO	1.05	1	(mA)
V5REF	5	1	(mA)
V5REF_Sus	5	1	(mA)
Vcc3_3	3.3	0.266	
VccADAC3	1.05	1	(mA)
VccADPLLA	1.05	0.08	
VccADPLLB	1.05	0.08	
VccCore	1.05	1.3	
VccDMI	1.1	0.042	
VccIO	1.05	2.925	
VccASW	1.05	1.01	
VccSPI	3.3	0.020	
VccDSW3_3	3.3	2	(mA)
VccDFTERM	1.8	0.19	
VccSus3_3	3.3	0.097	
VccSusHDA	3.3	1	(mA)
VccVRM	1.5	0.16	
VccCLKDMI	1.05	0.02	
VccSSC	1.05	0.095	
VccDIFFCLKN	1.05	0.055	
VccALVDS	3.3	1	(mA)
VccTX_LVDS	1.8	0.06	



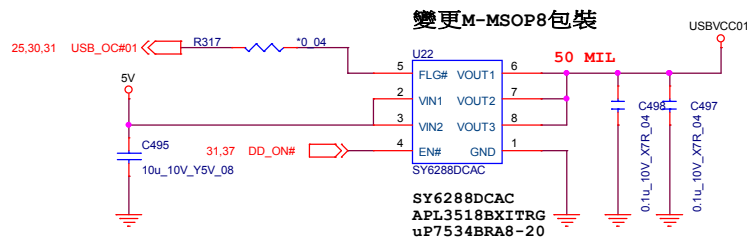
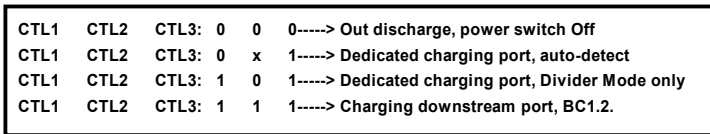
藍天電腦 CLEVO CO.

Title	[28] Lynx 9/9-CLK/GND		
Size	Document Number	6-71-W65J0-D01	Rev 1.0
Custom	6-7P-W65J4-001		
Date:	Wednesday, October 09, 2013	Sheet 28 of 46	

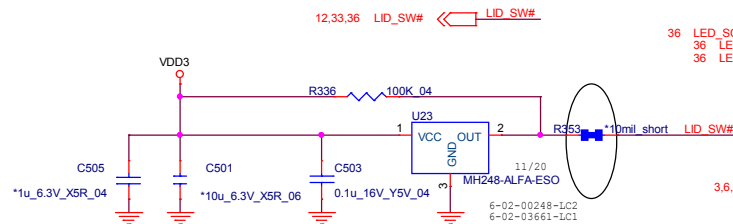
17,20,21,22,24,26,27,29,30,32,33,36,37,38,39,43  
2,3,12,17,20,24,25,29,31,33,35,37,38,40,42  
3,6,9,10,11,12,19,20,21,22,23,24,26,27,29,30,31,32,33,34,35,36,37,41



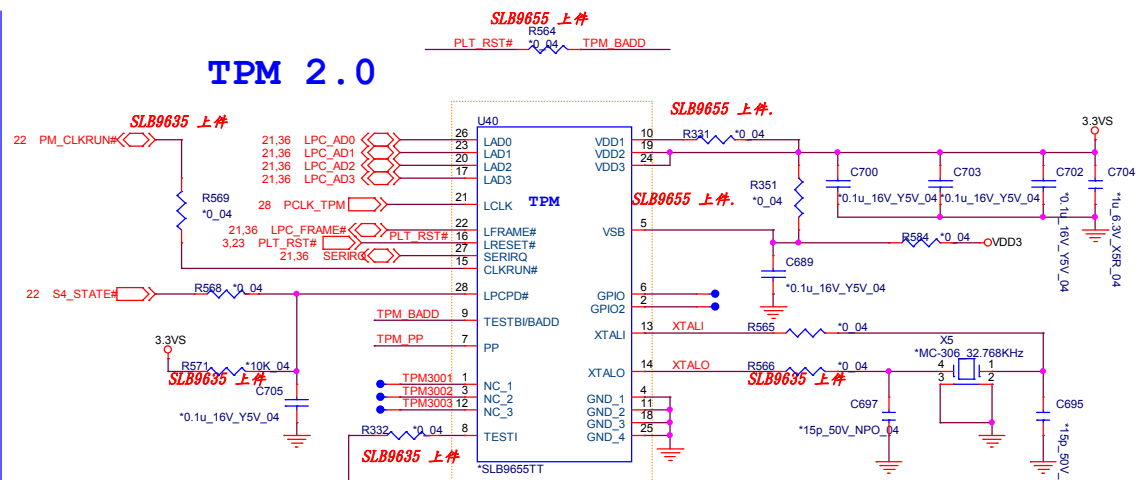
## Co-lay



## LID



**FOR POWER SWITCH BOARD**

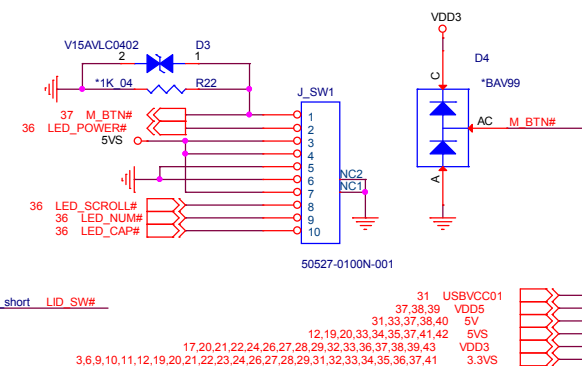
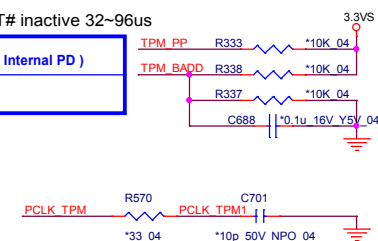


Asserted before entering S3

LPC reset timing:

LPCPD# inactive to LRST# inactive 32~96us

TPM_PP	HI: ACCESS LOW: NORMAL ( Internal PD )
TPM_BADD	HI: 4E/ 4F H LOW: 2E/ 2F H

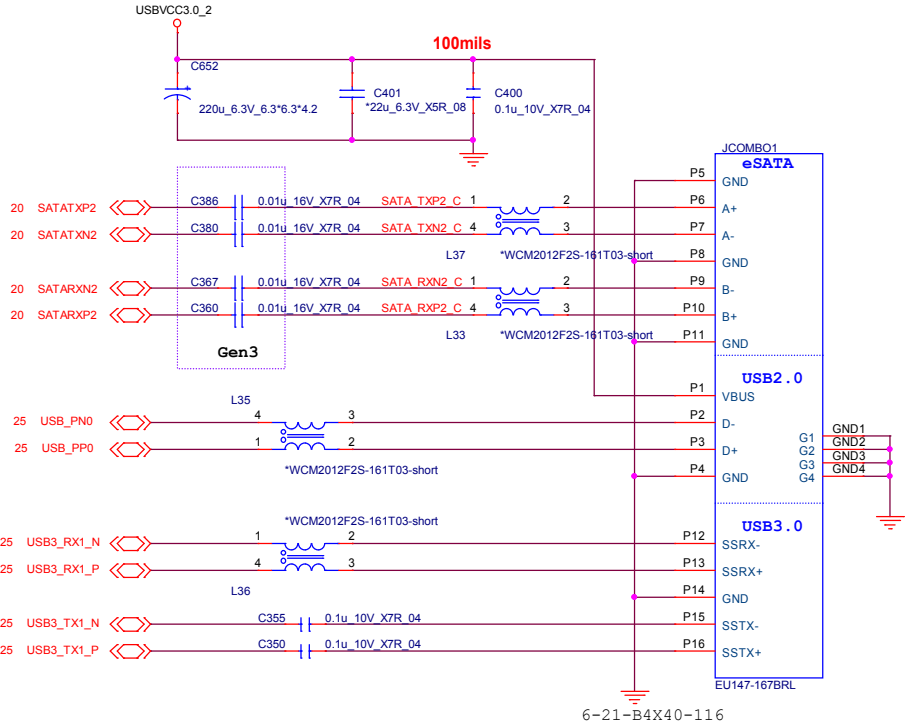


藍天電腦 CLEVO CO.

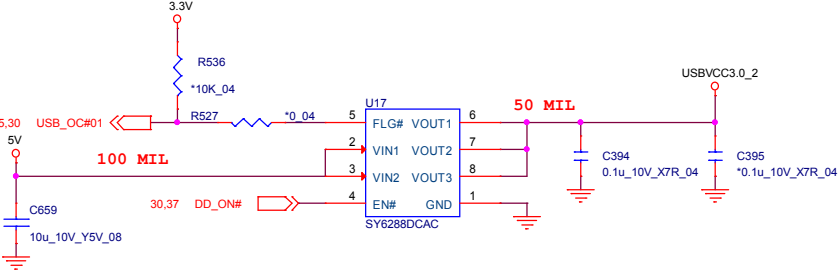
Title	[30]USB charge,CCD,TPM,POWER CON
-------	----------------------------------

Size	Document Number	Rev
Custom	6-7P-W65J4-001	1.0
6-71-W65J0-D01		
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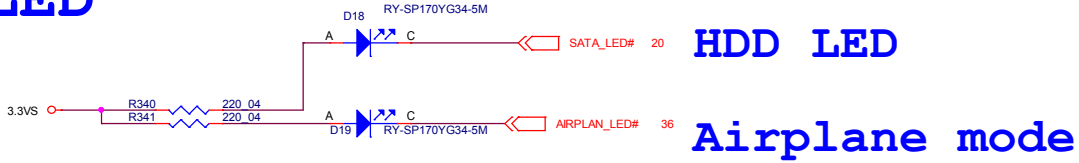
ESATA+USB3.0 USB3.0 PORT(PORT1)



USB POWER SWITCH

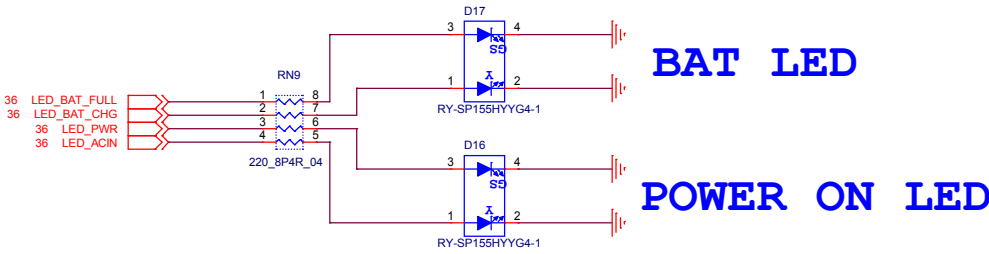


LED

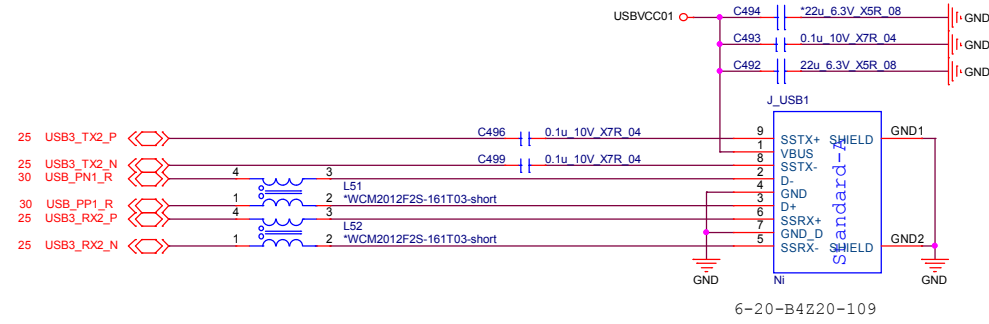


WLAN/BLUETOOTH LED

	WLAN LED
Windows 7	WLAN ON 亮
	WLAN OFF 不亮
Windows 8	Airplane ON 亮
	Airplane OFF 不亮

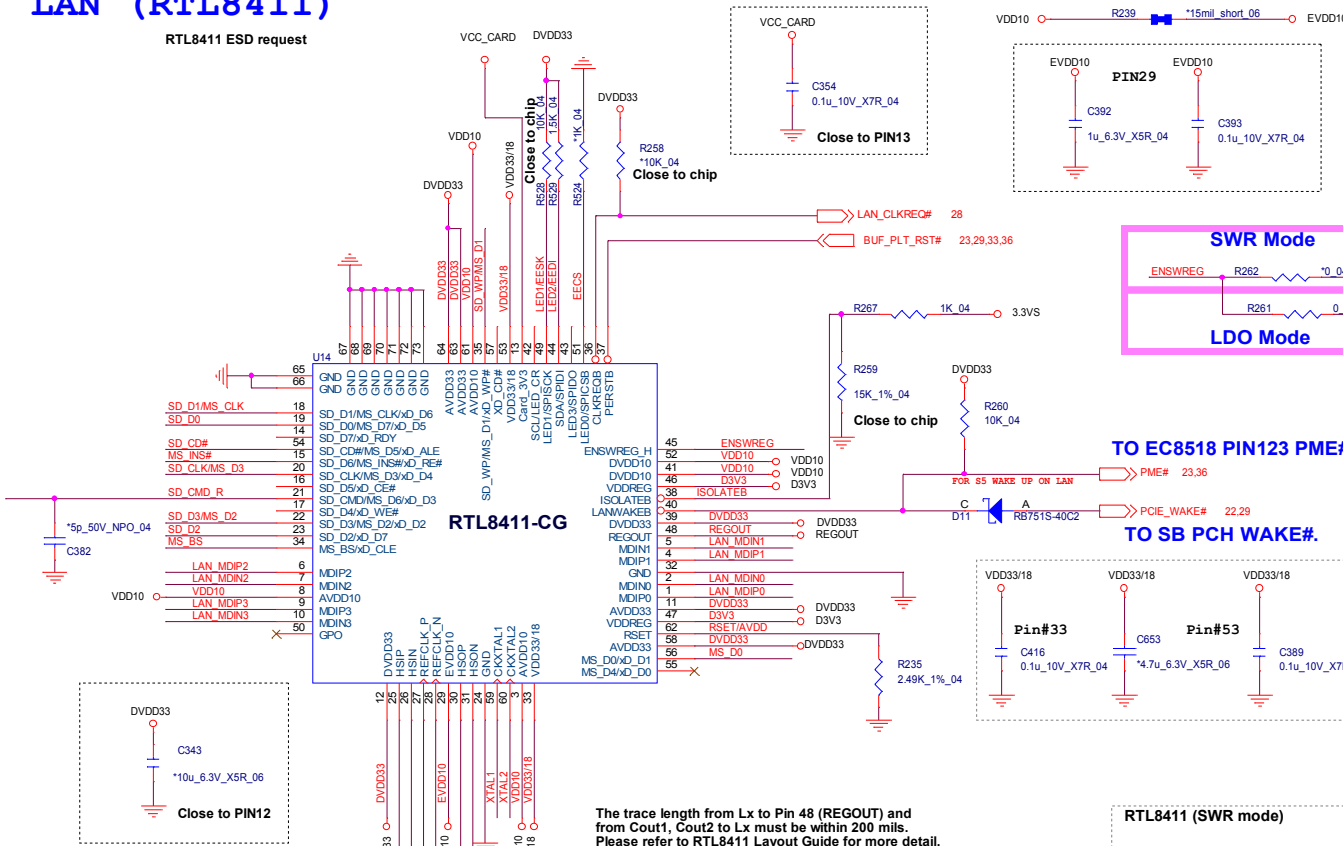


USB3.0 PORT(PORT3)



# LAN (RTL8411)

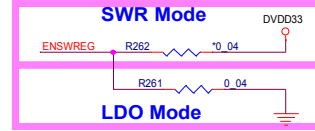
RTL8411 ESD request



The trace length from Lx to Pin 48 (REGOUT) and from Cout1, Cout2 to Lx must be within 200 mils. Please refer to RTL8411 Layout Guide for more detail.

C419 & C424 capacitors must be close to pin side

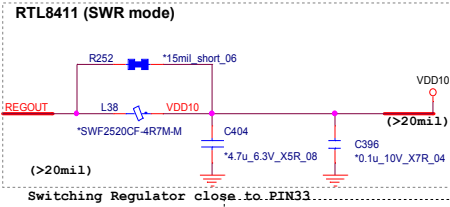
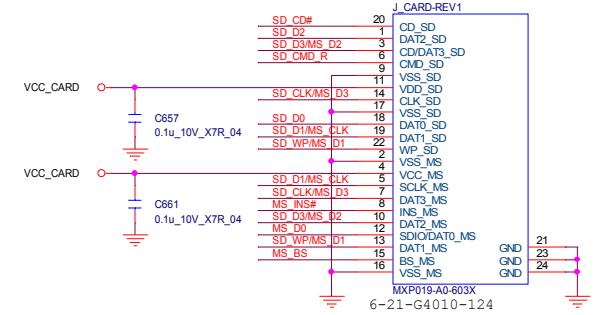
Close to PIN13



TO EC8518 PIN123 PME#.

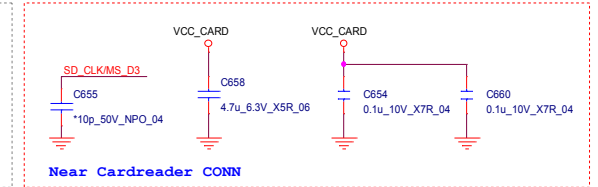
TO SB PCH WAKE#.

4 IN 1 SOCKET SD/MMC/MS/MS Pro CO-LAY W650SR



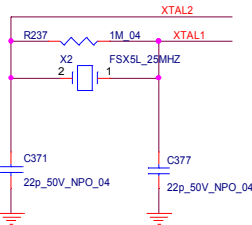
Switching Regulator close to PIN33

DVDD33 rise time must be controlled between 1mS and 100mS

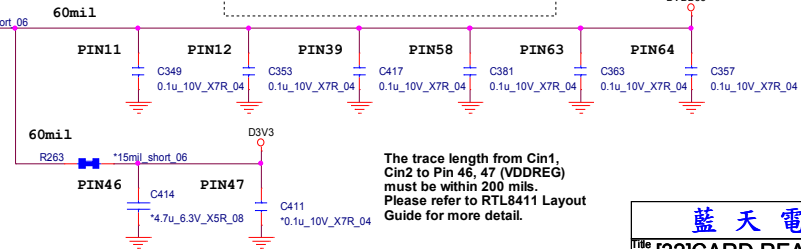
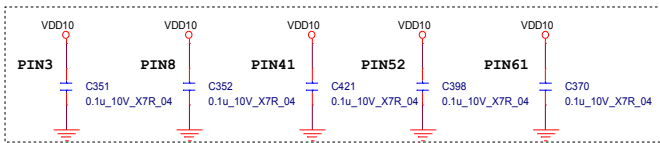


Near Cardreader CONN

Crystal 8045 & 3225 Co-lay



meet falling time <1ms

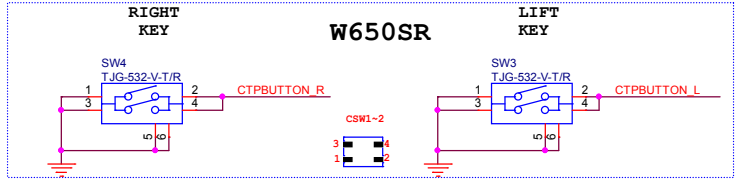
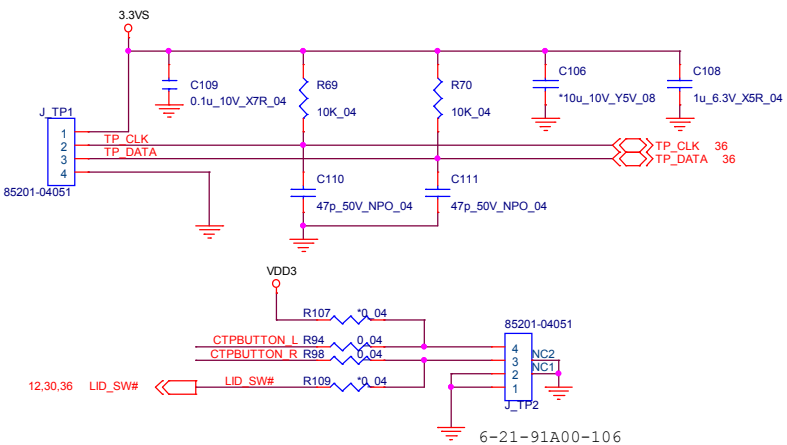


The trace length from Cin1, Cin2 to Pin 46, 47 (VDDREG) must be within 200 mils. Please refer to RTL8411 Layout Guide for more detail.

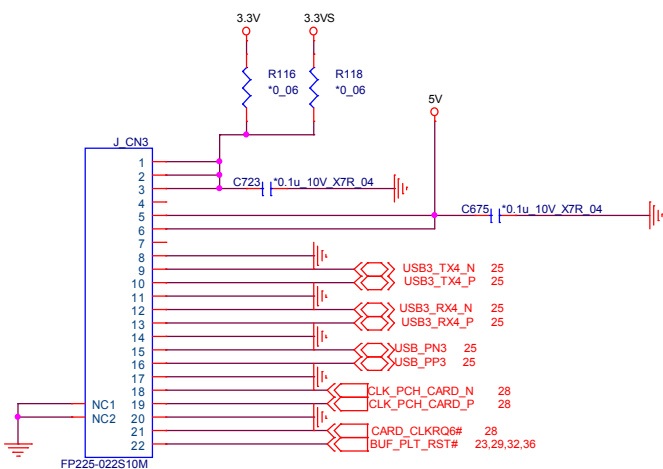
藍天電腦 CLEVO CO.			
[32]CARD READER/ LAN RTL8411			
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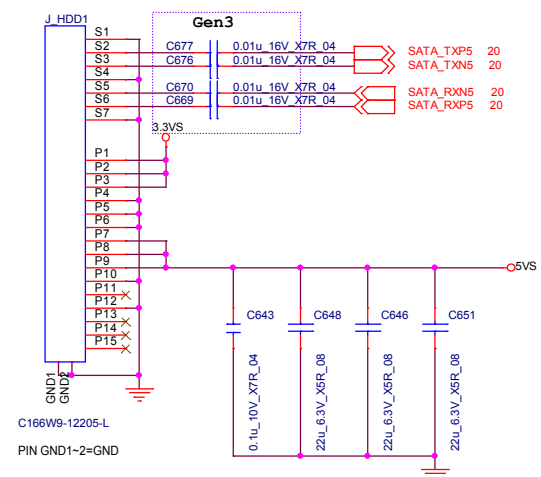
CLICK TP



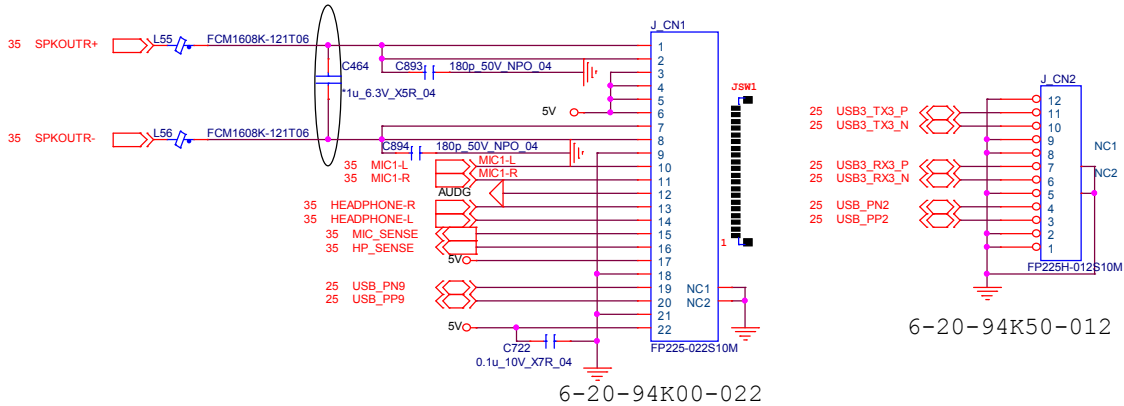
6-53-3050B-042 100g



HDD CONNECT1 (MASTER)



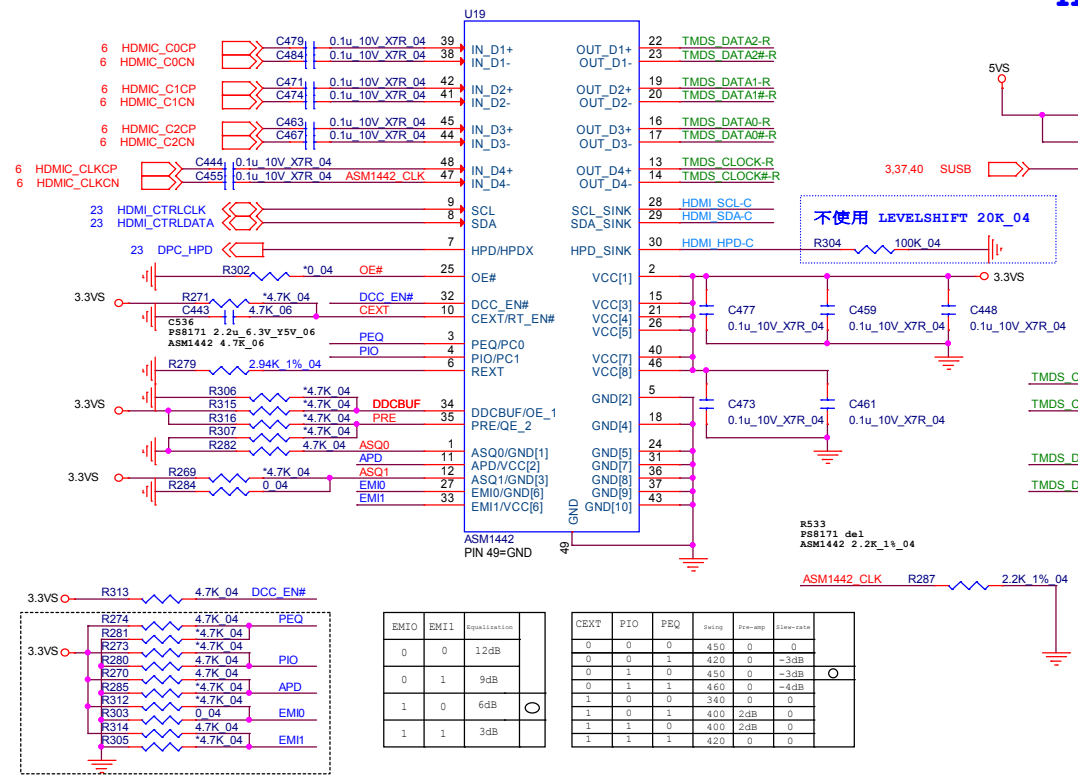
FOR AUDIO BOARD



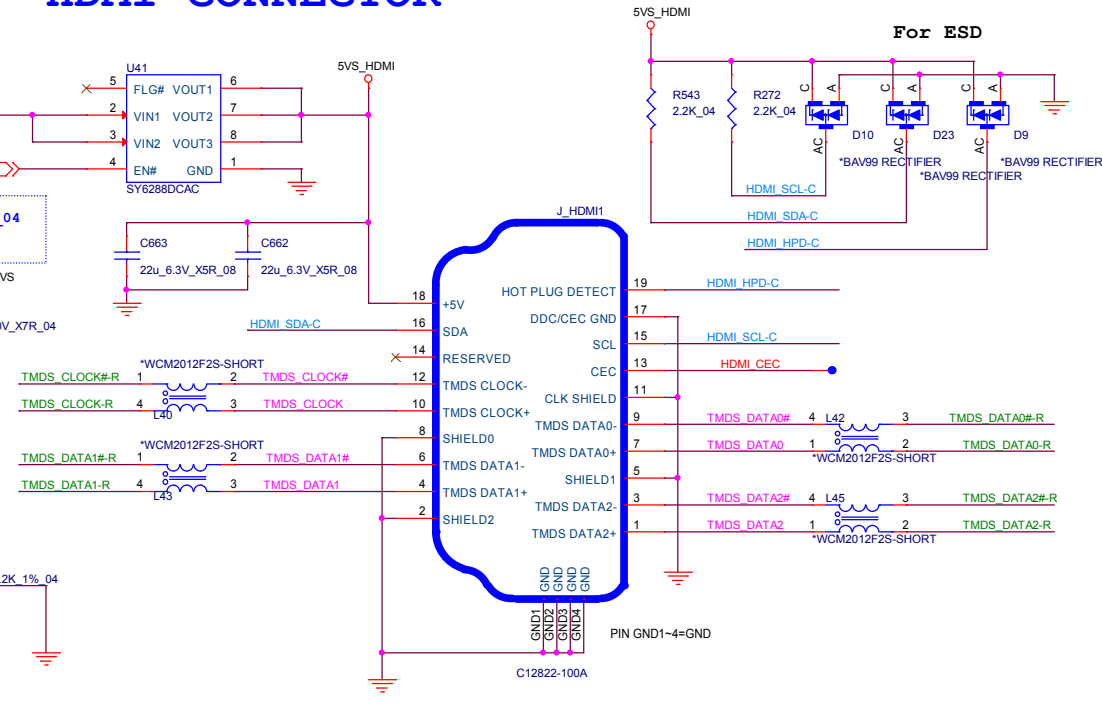
30,31,37,38,40 5V  
12,19,20,30,34,35,37,41,42 5VS  
17,20,21,22,24,26,27,28,29,30,32,36,37,38,39,43 VDD3  
2,3,12,17,20,24,25,28,29,31,35,37,38,40,42 3.3V  
3,6,9,10,11,12,19,20,21,22,23,24,26,27,28,29,30,31,32,34,35,36,37,41 3.3VS

藍天電腦 CLEVO CO.			
Title [33]HDD,CLICK TP,AUDIO CON,USB3.0 REDRIVER			
Size A3	Document Number 6-7P-W65J4-001	6-71-W65J0-D01	Rev 1.0
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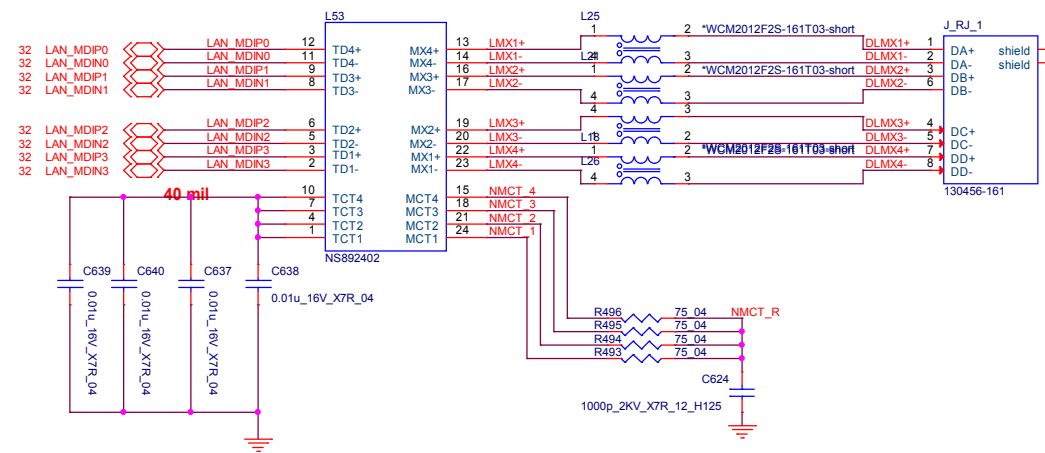
# HDMI LEVEL SHIFT



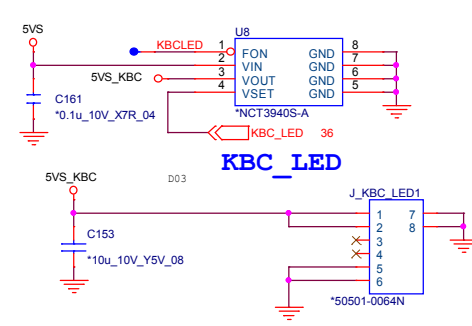
# HDMI CONNECTOR



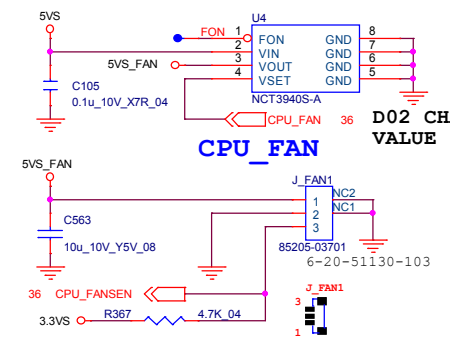
# GIGA LAN (RTL8411) LAN POART



# KBC LED CONTROL



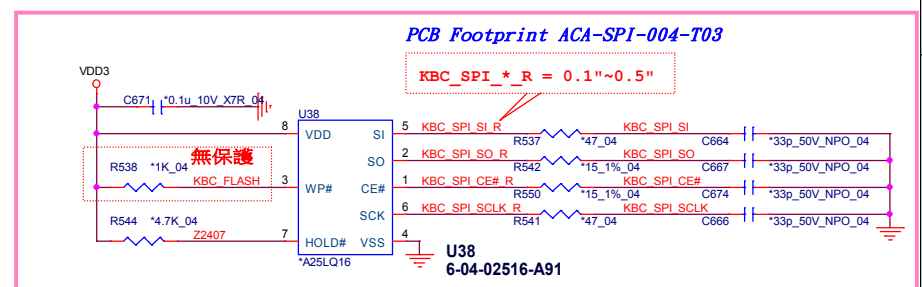
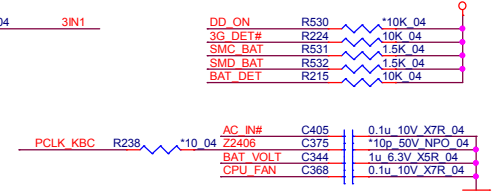
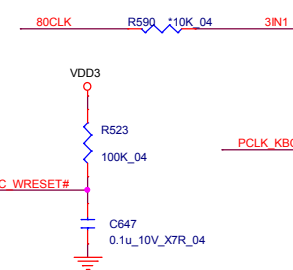
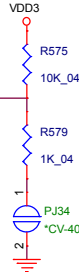
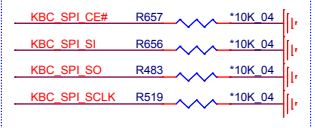
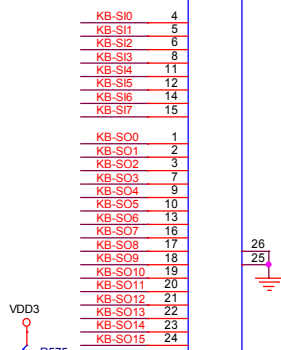
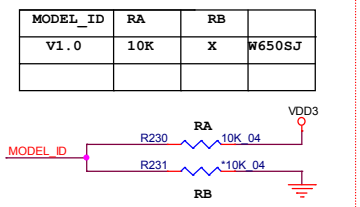
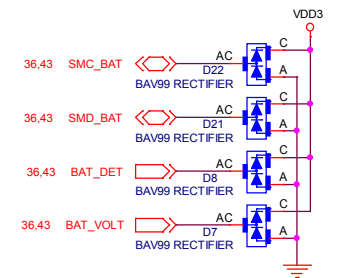
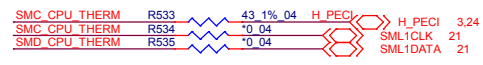
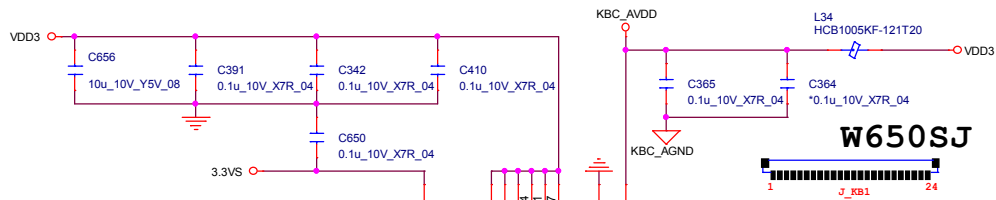
# CPU FAN CONTROL



PD# Control      AZ\_RST# For 3.3V  
HDA Link De-pop



12,19,20,30,33,34,35,37,41,42 5V  
12,19,20,30,33,34,35,37,41,42 5V  
2,3,12,17,20,24,25,28,29,31,32,33,34,36,37,41 3.3V  
3,6,9,10,11,12,19,20,21,22,23,24,26,27,28,29,30,31,32,33,34,36,37,41 3.3V



藍天電腦 CLEVO CO.			
[36]KBC-ITE IT8587			
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6-03-08587-FX

Windows 8	Airplane ON	亮
	Airplane OFF	不亮

17,20,21,22,24,25,28,29,30,32,33,37,38,39,43  
2,3,12,17,20,24,25,28,29,31,33,35,37,38,40,42  
3,6,9,10,11,12,19,20,21,22,23,24,26,27,28,29,30,31,32,33,34,35,37,41



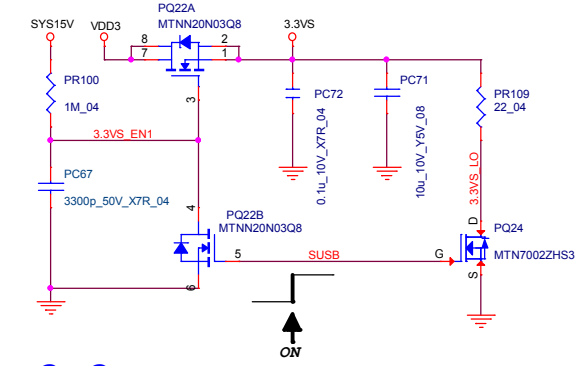
## DD\_ON#

## SUSB

## SLP\_A

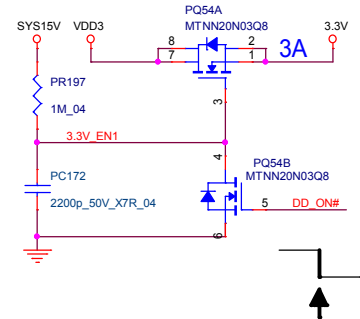
## 3.3VS

NMOS



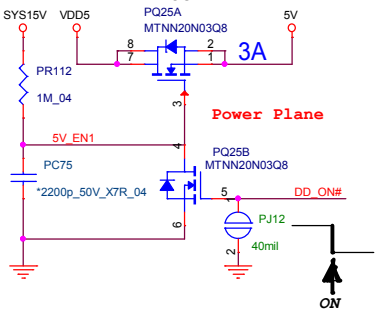
## 3.3V

NMOS



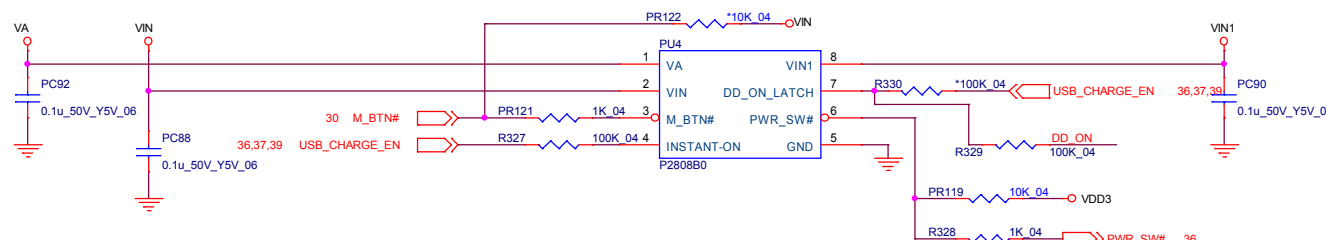
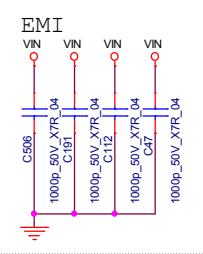
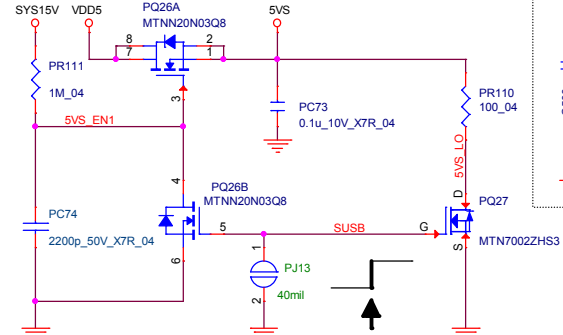
## 5V

NMOS



## 5VS

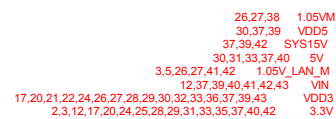
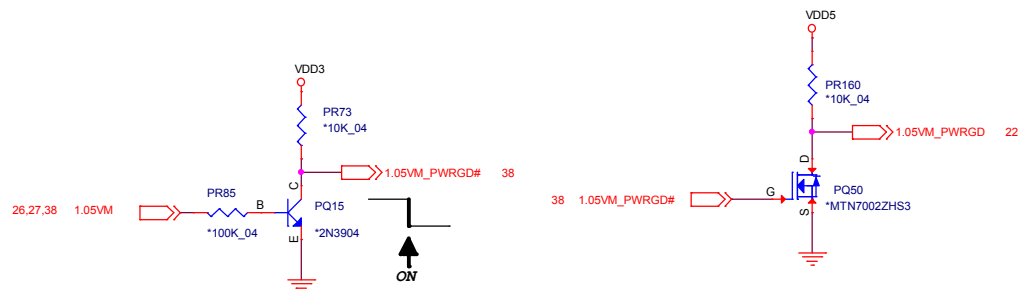
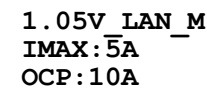
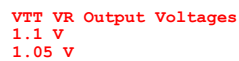
NMOS



- 43 VA
- 39 VIN1
- 30,38,39 VDD5
- 38,39,42 SYS15V
- 30,31,33,38,40 5V
- 12,38,39,40,41,42,43 VIN
- 12,19,20,30,33,34,35,41,42 5VS
- 17,20,21,22,24,26,27,28,29,30,32,33,36,38,39,43 VDD3
- 2,3,12,17,20,24,25,28,29,31,33,35,38,40,42 3.3V
- 3,6,9,10,11,12,19,20,21,22,23,24,26,27,28,29,30,31,32,33,34,35,36,41 3.3VS

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Title		[37] 5VS,3VS,3.3VM,1.5VS_CPU	
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Title [38]1.05V series			
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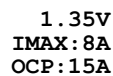
VDD3



Title			
[39]VDD3, VDD5			
Size A3	Document Number	Rev	
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37 VIN1  
37,38,42 SYS15V  
30,37,38 VDD5  
12,37,38,40,41,42,43 VIN  
17,20,21,22,24,26,27,28,29,30,32,33,36,37,38,43 VDD3

VDDQ\_VTT

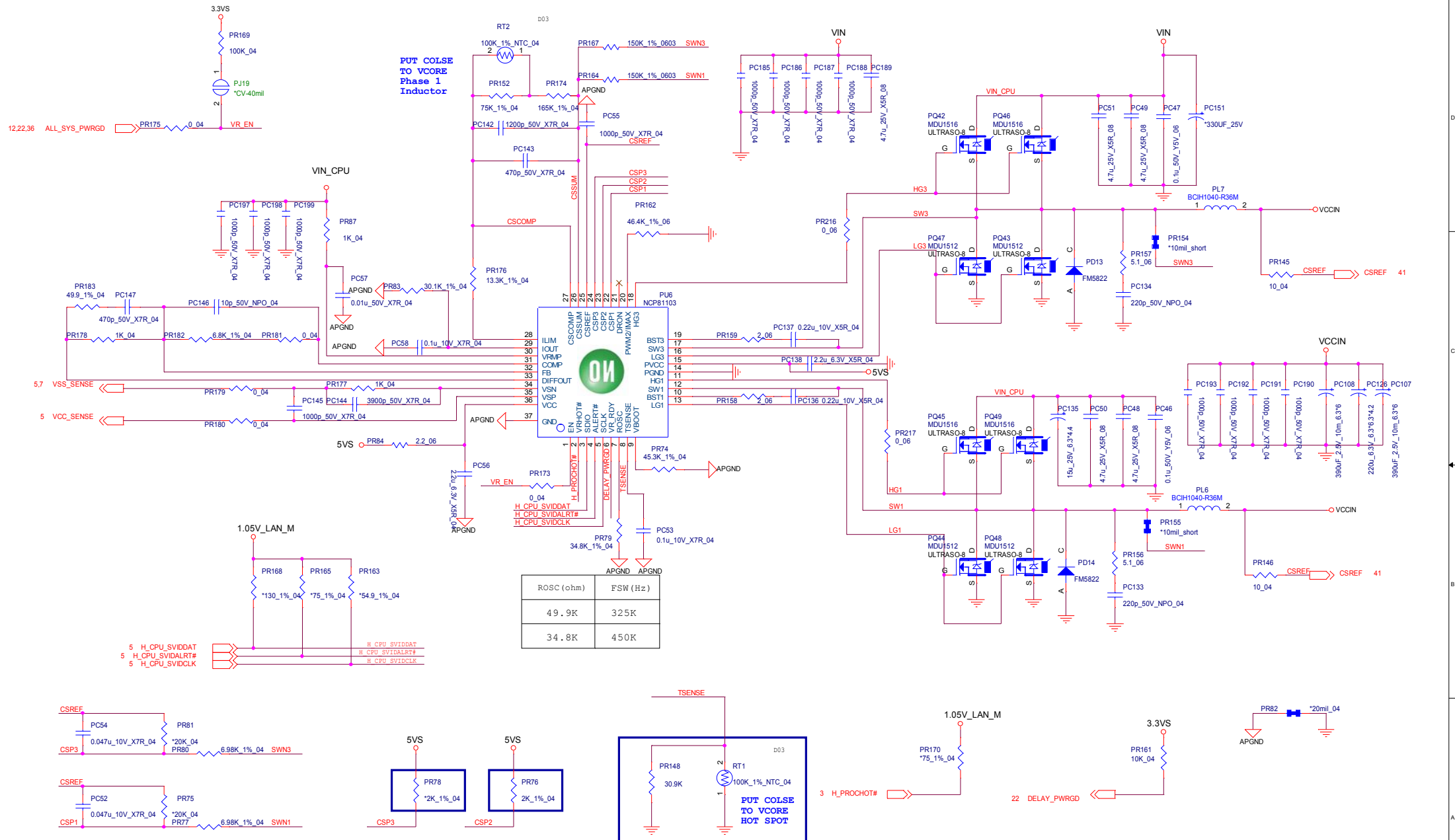


1.35V  
ICC MAX VDDQ=4.2A

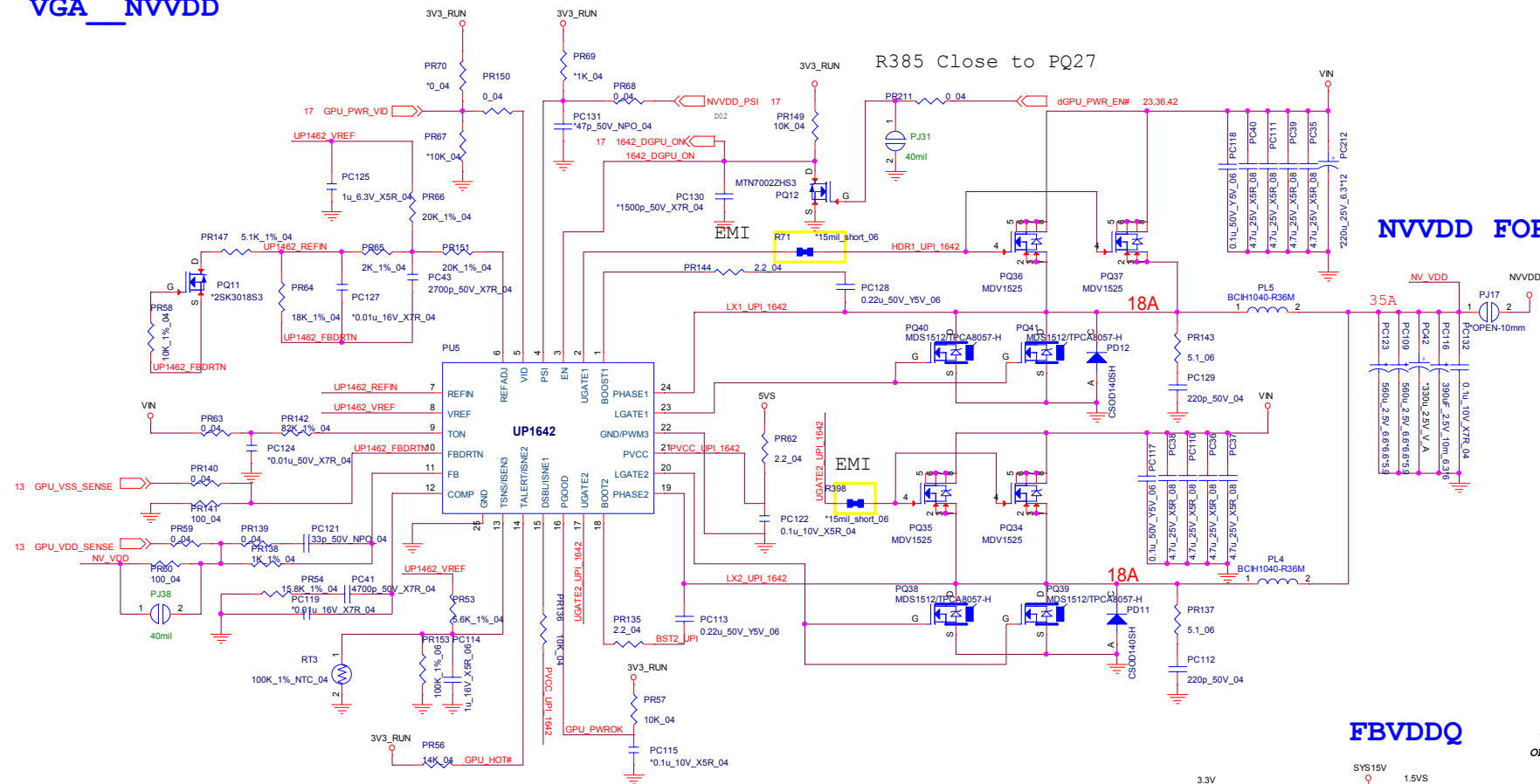
1.5VS  
IMAX:5A  
OCP:10A

<div style="text-align: center;">    <b>藍 天 電 腦 CLEVO CO.</b> </div>			
<b>Title</b> [40]DDR 1.5V or 1.35V/0.75VS/1.5VS			
<b>Size</b> <b>Custom</b>	<b>Document Number</b>		<b>Rev</b> <b>1.0</b>
	<b>6-71-W65J0-D01</b>		
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# VGA\_\_NVVDD

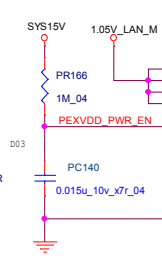
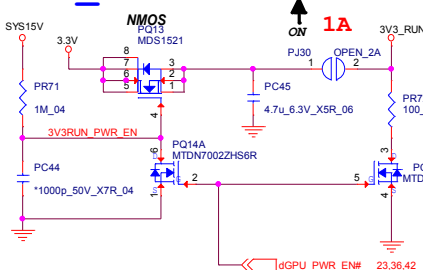


## NVVDD FOR N14\_VGA

## FBVDDQ

## 3V3\_RUN

## PEX\_VDD



1.05V@4A  
250 MIL

6-01-74132-Q61

藍天電腦 CLEVO CO.

Title [42]N14P,NVVDD,PEX,FBVDDQ

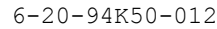
Size Custom Document Number 6-71-W6500-D03 Rev 3.0

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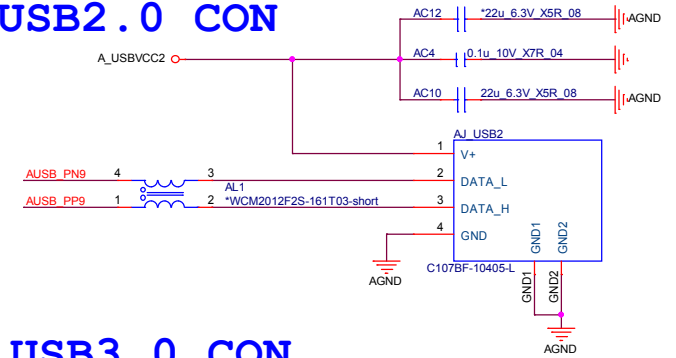


Figure 1 shows the chemical structures of six compounds: 1AR, 2AR, 3AR, 4AR, 5AR, and 6AR. Each structure is a 10-membered ring with a carbonyl group at position 1 and a methyl group at position 10. The structures are labeled 1AR through 6AR, with a '0.04' label next to each.

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USB2.0 CON



**USB Interface Circuit Schematic**

**Module: C19007-90905-L NEW**

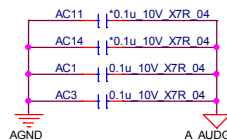
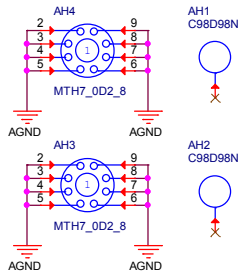
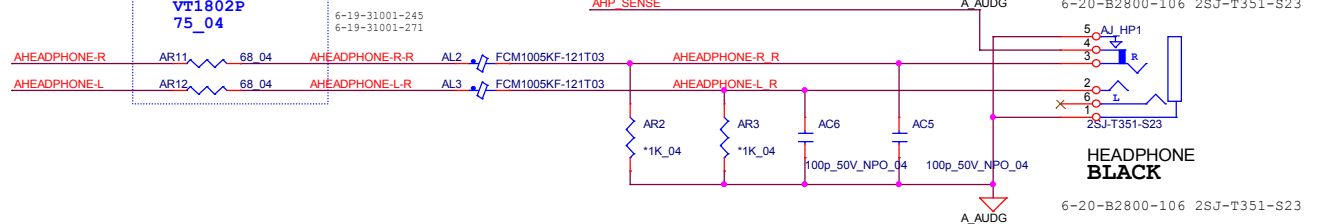
**Key Components:**

- Capacitors: 22uF 6.3V XSR\_08, 0.1uF 10V X7R\_04 (multiple)
- Resistors: 100u 6.3V B A
- Module Pins: AUSB3 TX3 P, AUSB3 TX3 N, AUSB PN2, AUSB PP2, AUSB RX3 P, AUSB RX3 N, AGND
- Module Labels: WCM2012F25-161T03-short 4, AL7, AL6, WCM2012F25-161T03-short 5

**Connections:**

- A\_USBVCC1 is connected to the module's power supply.
- AC27, AC31, and AC32 are connected to the module's power supply.
- AC26 and AC25 are connected to the module's power supply.
- AUSB3 TX3 P, AUSB3 TX3 N, AUSB PN2, AUSB PP2, AUSB RX3 P, and AUSB RX3 N are connected to the module's data lines.
- AGND is connected to the module's ground.

Resistor 32 or 33\_04  
meet WLK Test  
VT1802P  
75 04



Title	[44]AUDIO BOARD
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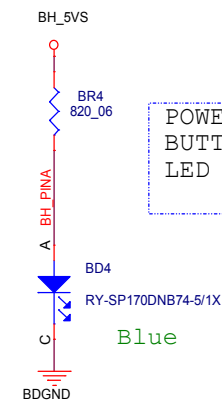
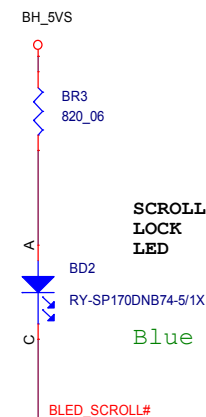
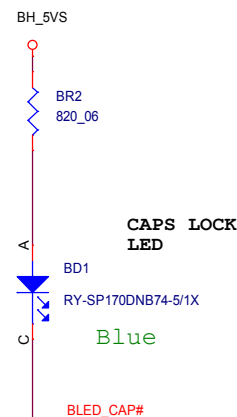
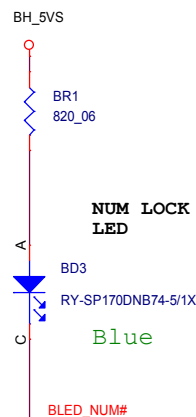
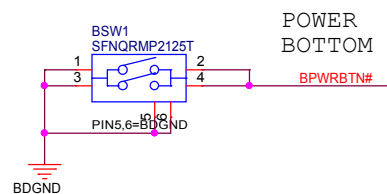
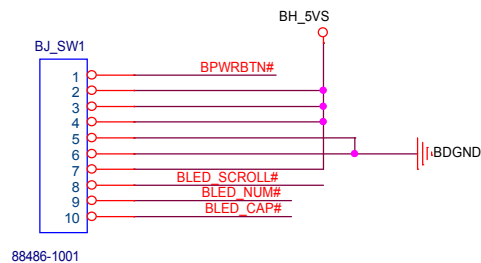
Size A3	Document Number <b>6-71-W6508-D06</b>	Rev 1.0
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# POWER & LED BOARD

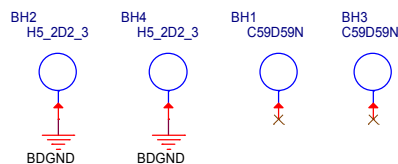
## 6-71-W650S-D04

1BR 820\_06  
2BR 820\_06  
3BR 820\_06  
4BR 820\_06  
5BR 820\_06  
6BR 820\_06

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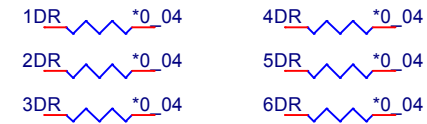
POWER  
BUTTON  
LED



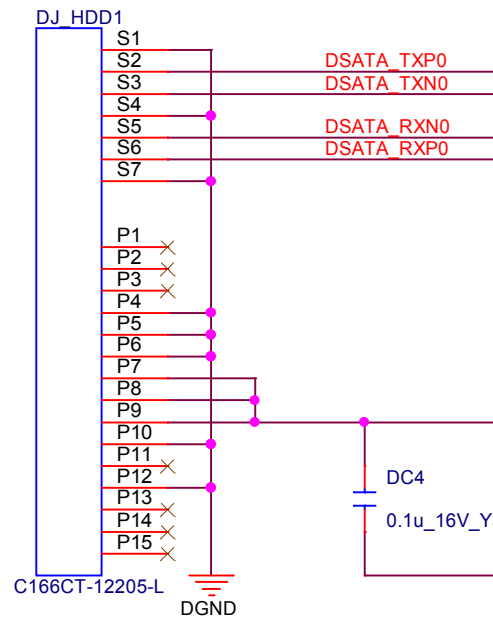
藍天電腦 CLEVO CO.

Title [45]POWER SWITCH BOARD		
Size Custom	Document Number 6-71-W650S-D04	Rev 1.0
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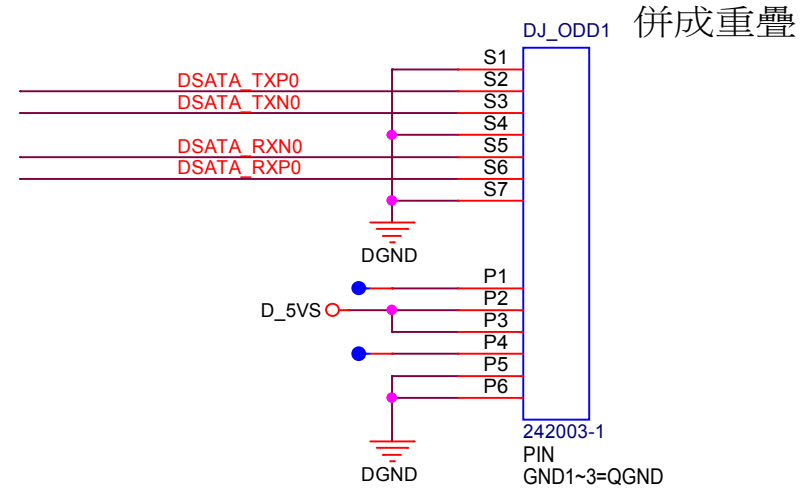
# 6-71-W650N-D04



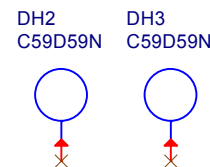
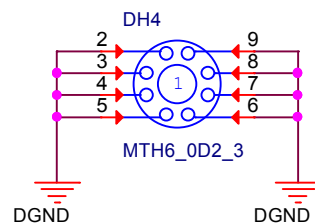
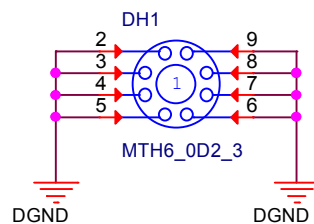
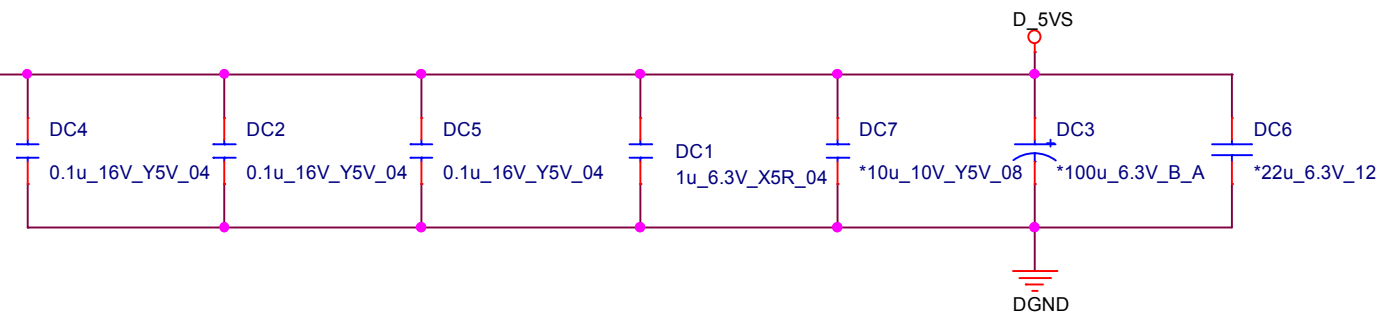
ODD TO HDD BOARD



6-21-C2710-122



6-21-14030-013



藍天電腦 CLEVO CO.

Title [46]ODD TO HDD BOARD

Size A Document Number 6-71-W650N-D04 Rev 1.0

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